

Four-Terminal RF Phase Change Switches: Design, Optimization and Fabrication

Submitted in partial fulfillment of the requirements for

the degree of

Doctor of Philosophy

in

Electrical and Computer Engineering

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December 2015

Table of Contents

Acknowledgements	5
Abstract	7
Chapter 1: Introduction	9
1.1 Motivation	9
1.2 RF Switch Technologies	10
1.3 Phase Change History and Physics	13
1.4 RF Phase Change Switches	16
1.5 Thesis Outline	20
Chapter 2: Phase Change RF Switch Design Considerations and Impact on Efficacy	22
2.1 Abstract	22
2.2 Introduction	22
2.4 Model Setup	26
2.5 Simulations of 3D Model vs. Measurement Results	30
2.6 3D Model vs. 2D Model	32
2.7 Simulation Results of Design Parameter Sweep	34
2.8 Summary	46
Chapter 3: Phase Change RF Switch Fabrication	48
3.1 Abstract	48
3.2 Introduction	48
3.3 Standard Switch Process Flow	49
3.4 Notched Switch Process Flow	54

3.5 Low Resistivity Tungsten Heater.....	56
3.6 AlN Barrier Layer	61
3.7 Low Resistivity GeTe	62
3.8 GeTe Contact Resistance	65
3.9 Summary	67
Chapter 4: DC Switch Characterization.....	68
4.1 Abstract	68
4.2 Introduction.....	68
4.3 DC measurement Test Setup.....	69
4.4 AlN Thickness Study, 105 nm vs. 170 nm	70
4.5 The Effect of RF Gap.....	77
4.6 GeTe 100 nm Thick	81
4.7 AlN 200 nm Thick	89
4.8 Summary	91
Chapter 5: RF Switch Characterization	93
5.1 Abstract	93
5.2 Introduction.....	93
5.3 One-Port S-Parameter Measurement Setup	94
5.4 AlN Thickness Study, 105 nm vs. 170 nm	97
5.5 The Effect of RF Gap.....	98
5.6 Two-Port S-Parameter Measurement Setup.....	99

5.7 GeTe 100 nm Thick	103
5.8 AlN 200 nm Thick	113
5.9 Switch Dimension Comparison	116
5.10 Summary	120
Chapter 6: Integration with RF CMOS Circuits	122
6.1 Abstract	122
6.2 Introduction	122
6.3 Flip Chip Solder Bump Bonding Process	123
6.4 LC-VCO	128
6.5 3/5 GHz LNA	129
6.6 Summary	135
Chapter 7: Conclusions and Outlook	136
7.1 Conclusions	136
7.2 Future Work	138
7.3 Contributions and Publications	140
Appendix	143
References	152

Acknowledgements

I would first like to thank my advisor, Prof. Jim Bain, for his continuous support and patience during my Ph.D research. His immense knowledge and positive thinking encouraged me even when I thought all hope was lost. I would also like to thank my co-advisor, Prof. Ed Schlesinger. Although he was extremely busy, he helped me advance my research with both his knowledge and financial support. In addition, I want to express appreciation to the other committee members, Prof. Jeyanandh Paramesh and Dr. Rob Young. They continuously demonstrated a vested interest in my success and provided feedback on my research throughout the project.

I would also like to thank DARPA (Defense Advanced Research Projects Agency) as this work was supported, in part, by the Defense Advanced Research Projects Agency RF-FPGA program under contract HR0011-12-C-0095 and, in part, by an ONR DURIP equipment grant, Grant #N000141310874. I appreciate the efforts of Prof. Jim Bain who worked to obtain funding from the ONR DURIP equipment grant to purchase the AJA sputtering chamber. That chamber was vital to the success of my Ph.D research. Without it, I could not have achieved the high quality W and GeTe that were required to build a working switch.

I would also like to thank my fellow students who I had the pleasure of working with during my time in the MISCIC and RF-FPGA project. Mohammad Noman offered many words of wisdom during the first few years of my Ph.D studies and valuable advice regarding strategies that would enable me to complete my degree. I would like to express appreciation to my office mates, Min Xu, Abhishek Sharma and Nabil El-Hinnawy for our amazing discussions on phase change and threshold switching phenomenon. In addition, I would like to thank the CMU Nanofab staff members Chris Bowman, Carsen Klien, Dr. Matt Moneck and Norm Gottorn for their help with the equipment in the cleanroom.

Last, but not least, I would like to thank my family and friends of their continuous support over this long, tortuous journey. I would like to thank my parents, Howard and Judy Slovin, for their emotional and financial support. I also appreciate the time my mom spent reading and reviewing my thesis. I would also like to thank my sister, Dr. Sara Slovin, and my girlfriend, Ms. Melody Albarran, who were continuously supportive of me.

Abstract

The programmability of the optical and electrical characteristics of chalcogenide PC materials using joule heating makes them useful for data storage and memory applications. This work explored the use of PC materials in RF switches. A 4-terminal RF PC switch that used a separate tungsten micro-heater to program the PC material was designed, optimized, fabricated and integrated with an RF CMOS circuit.

RF switches require a low ON-state resistance ($< 1 \Omega$) while maintaining a high ON-OFF ratio (10^4). A low resistivity ($1.5 \times 10^{-6} \Omega\text{-m}$) PC material, GeTe, was developed to achieve an ON-state resistance of 1Ω . The use of an AlN high thermal conductivity barrier layer was also introduced to improve the RF isolation and reduce the OFF-state capacitance (C_{OFF}) to as low as 10 fF. These improvements in the materials enabled an RF switch cutoff frequency (F_{CO}) of 9.6 THz.

The effects of RF gap length and AlN barrier layer thickness on the RF performance were also explored in detail. Reducing the RF gap length, from 900 nm to 400 nm, increased the F_{CO} from 4.5 THz to 7.2 THz despite an increase in C_{OFF} from 11.7 fF to 15.4 fF. Increasing the AlN barrier layer thickness also improved the RF performance of the switch by reducing the capacitance attributed to the presence of the heater; however, this was at the cost of increasing MPA. Measurement results showed that increasing the AlN thickness above 170 nm does not further reduce C_{OFF} (10 fF). Therefore, increasing the AlN thickness any further only results in an increase in MPA with no additional improvement in F_{CO} .

These switches were also integrated with a CMOS low-noise amplifier (LNA) using a custom flip chip solder bump bonding process to allow for *in-situ* reconfiguration between the 3 GHz and 5 GHz modes. The gain of the 3/5 GHz LNA was not significantly affected by the presence of the switch and solder bumps. It was approximately 20 dB in both modes of operation. The noise figure of the LNA in the 3 GHz mode increased from 1.9 dB to 2.85 dB due to the presence of the switch and solder bumps.

However, 0.65 dB can be attributed to the solder bumps, resulting in the switch only degrading the noise figure of the LNA by 0.3 dB.

Chapter 1: Introduction

1.1 Motivation

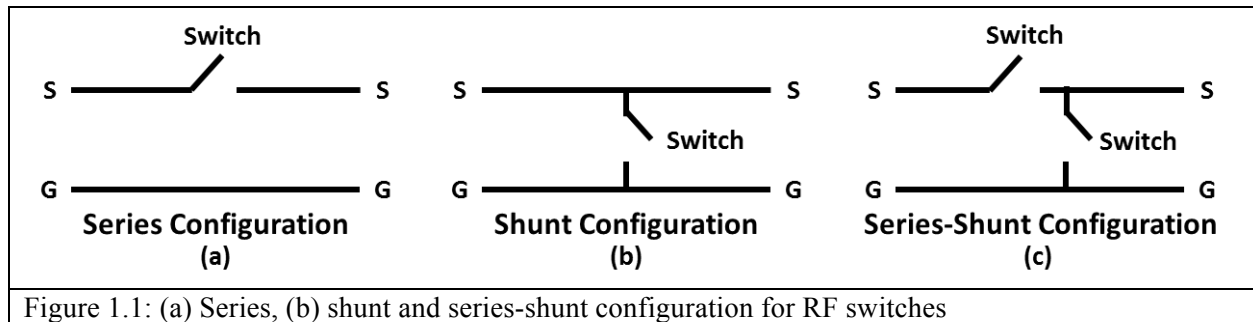
Wireless communication is all around us, from cellular phones to satellite television, and most people come into contact with it every day. Data can be transmitted to our phones, computers, cars and televisions using radio frequencies. Specialized electronic circuits (Radio Frequency (RF) circuits) are used to transmit and receive this wireless data which allows us to perform such diverse activities as transmitting personal location information to a network of satellites to checking the scores of last night's basketball games on our smart phone while walking the dog. There are over 25 radios in the iPhone 6 that are used for various cellular bands (i.e. 3G, LTE), WiFi, GPS, Bluetooth and more. Each wireless communication standard requires its own special radio that is designed for a small band of frequencies at which that standard operates. There are 44-frequency bands that are used for the LTE wireless standard [1]. However, the iPhone 6 from AT&T only has the ability to operate on 16 to 20 of those bands due to the space the necessary radio occupies for each band [1]. A single narrow band RF circuit is used to for each frequency band because the incoming signals are at frequencies in the gigahertz range, only operate with a few pico-Watts of power and are at the same time being mixed with many other RF signals [1]. Due to these factors, a single wideband RF circuit cannot be used to achieve the required performance to operate at these wireless standards.

A great solution for space limitations inherent in wireless devices would be designing a switch that would work for these high frequency signals and would allow for the re-configurability of RF circuits that would otherwise not be possible. Some of these switches are already present in our smart phones, enabling the hardware to switch an antenna between transmit and receive RF circuitries. Further integration of RF switches in RF circuits would allow for reconfigurable radios that could operate at numerous frequency bands while still maintaining high performance. By combining multiple radio

standards together, a smaller form factor can be achieved, thus reducing costs [1]. Reconfigurable radios would also allow users to have access to more wireless standards that otherwise would not be possible due to space constraints. RF switches could enable mobile devices to adapt to future radio standards thereby increasing the device's lifespan [2]. RF switches have already been demonstrated in many other RF components such as a reconfigurable inductors [3], LC-VCOs (inductive-capacitive voltage controlled oscillators) [4], antennas [5], phase shifters [6], power amplifiers (PA) [7] and LNAs (low noise amplifiers) [8].

1.2 RF Switch Technologies

The goal of an RF switch is to allow the RF signal to pass through when the switch is in the ON-state and block the RF signal when it is in the OFF-state. This can be done in one of three configurations: series, shunt and series shunt. In a series configuration (fig. 1.1(a)), the switching lies in the RF signal path. For a shunt configuration (fig. 1.1(b)), the switch turns on and off a shunt path to ground. When the switch is in the ON position, the RF signal is shunted to ground preventing the RF signal from propagating further. A series-shunt configuration (fig. 1.1(c)) combines both of these features to improve the RF performance. Two switches are used in conjunction to either allow the RF signal to pass through or to route the RF signal to ground.



This thesis will only demonstrate switches in the series configuration. The RF switch performance can be determined by measuring the insertion loss of the switch in the ON-state and the isolation of the switch in the OFF-state. The figure of merit of RF switches is their cutoff frequency (F_{CO})

using their ON-state resistance (R_{ON}) and OFF-state capacitance (C_{OFF}). The F_{CO} is defined as the frequency at which the magnitude of the switch impedance in the ON-state is equal to the magnitude of the switch impedance in the OFF-state ($1/(2\pi \times R_{ON} \times C_{OFF})$). RF switches require a low R_{ON} ($< 1 \Omega$) while maintaining a high ON-OFF ratio ($R_{OFF}/R_{ON} \geq 10^4$) and a low C_{OFF} (< 15 fF) for use in reconfigurable RF circuits. Some examples of working RF switch technologies are: MEMS (micro electrical-mechanical systems), PIN (p-type semiconductor, intrinsic semiconductor, n-type semiconductor) diodes, HEMTs (high electron mobility transistors), CMOS (complementary metal oxide semiconductor) and Phase Change (PC). The state of the art of each of these will be discussed below.

MEMS switches are voltage controlled and require large voltages to mechanically actuate a lever that makes mechanical and electrical contact. RF MEMS switches requires 20-80V to turn the switch on but uses little to no current while having a C_{OFF} of 2-4 fF [9]. An SP3T (single poll – triple throw) has been demonstrated using a 65 V actuation voltage with insertion loss of less than 0.8 dB and isolation over 25 dB up to 20GHz [10]. A shunt RF MEMS switch with actuation voltages of less than 15V has been demonstrated [11]. The MEMS switch lifetime can be as high as 7 billion cycles with an insertion loss of less than 0.1 dB and 20 dB of isolation up to 40GHz [11]. RF MEMS switches have been used to create 2 and 4-bit TTD phase shifters with an R_{ON} of approximately 1Ω [6]. RF MEMS switches have also been used to tune matching networks for a multiband LNA and PA [7]. Besides the large actuation voltage required to turn the switch on, another disadvantage is their large size as RF MEMS switches are typically a few hundred microns a side.

PIN diodes have also been used as RF switches [5], [12]. They act as a current controlled variable resistor with a higher bias current, which results in a lower R_{ON} . AlGaAs PIN diodes in a single pole double throw (SPDT) configuration have been shown to exhibit a 0.6 dB insertion loss and over 35 dB of isolation at 40 GHz [12]. The PIN diodes require 10 mA of bias current in the ON-state and - 5 V of bias in the OFF-state [12]. The AlGaAs PIN diodes can operate with up to 26 dBm of incident power [12]. PIN diodes have been used to reconfigure an annular slot antenna [5]. In this instance, two

PIN diodes were used to configure the impedance matching circuit allowing the antenna to operate at 5.2, 5.8 and 6.4 GHz [5]. Two downsides to PIN diodes are that they need constant current whenever the switch is on and, as it is a two-terminal device, the RF signal and programming current must share the same path. This may limit where the switch can be used to reconfigure RF circuits.

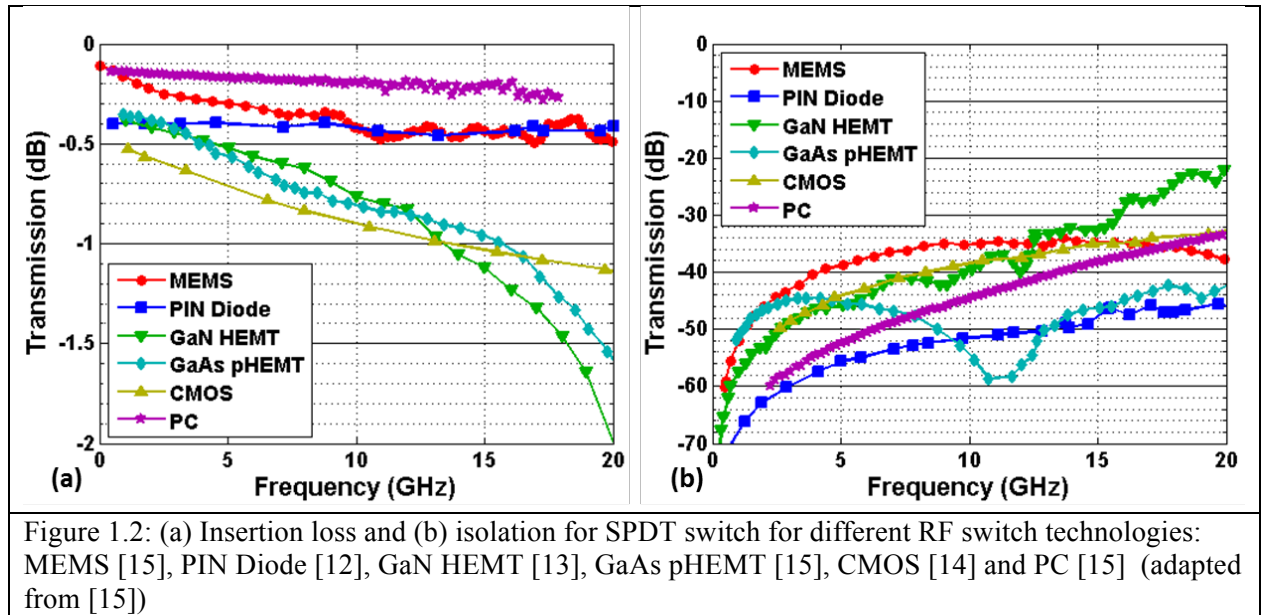
HEMTs are popular choices for use as an RF switch because of they have higher mobility than traditional CMOS technology (resulting in lower R_{ON}) and they have high power handling capabilities. A GaN HEMT on SiC has been demonstrated as an RF switch in an SPDT configuration that can handle large amounts of RF power [13]. A switch designed for frequency ranges from DC- 12 GHz has 1.0 dB of insertion loss and 16 dB of isolation and can up to handle 15 W of RF power [13]. These transistors are voltage controlled and have a pinch-off voltage of -4.2 V to turn the switch off [13].

Silicon analog hardware already exists in every system platform, therefore RF silicon switches are attractive due to their monolithic integration resulting in lower assembly costs. An SPDT using series shunt CMOS switches has been tested from DC to 60 GHz at the 45 nm node [14]. The switches were fabricated on an SOI substrate, to minimize substrate coupling, allowing for an insertion loss of 1.2 dB and an isolation of 33 dB at 20 GHz [14]. One major issue with RF CMOS switches is that, in order to reduce the R_{ON} of the switch to 1 Ω , an extremely wide device must be made. The resulting CMOS switch at the 45 nm node will have an F_{CO} of less than 2 THz [4].

RF switches using PC (chalcogenide) material have shown promising results. These switches use the resistance change between the crystalline (low resistance) and amorphous phases (high resistance) to turn the switch on and off, respectively. An SPDT using series shunt PC switches has been demonstrated to have an insertion loss of 0.2 dB and an isolation of 38 dB [15]. Unlike the other RF switches previously discussed, PC switches are non-volatile and only require power to switch between states, not to maintain a particular state. The transformation voltages can be as high as 19 V [16], but that can be reduced by sizing the device. These switches can be designed to be 4-terminal devices, thereby separating the control (programming) signal from the RF signal. This, in conjunction with their smaller

size (30 μm on a side), makes them a promising candidate for integration into RF circuits. RF PC switches have been used to reconfigure inductors [3], [17]. They have also been used to reconfigure a wide tuning range LC-VCO [4] and a 3/5 GHz LNA [8].

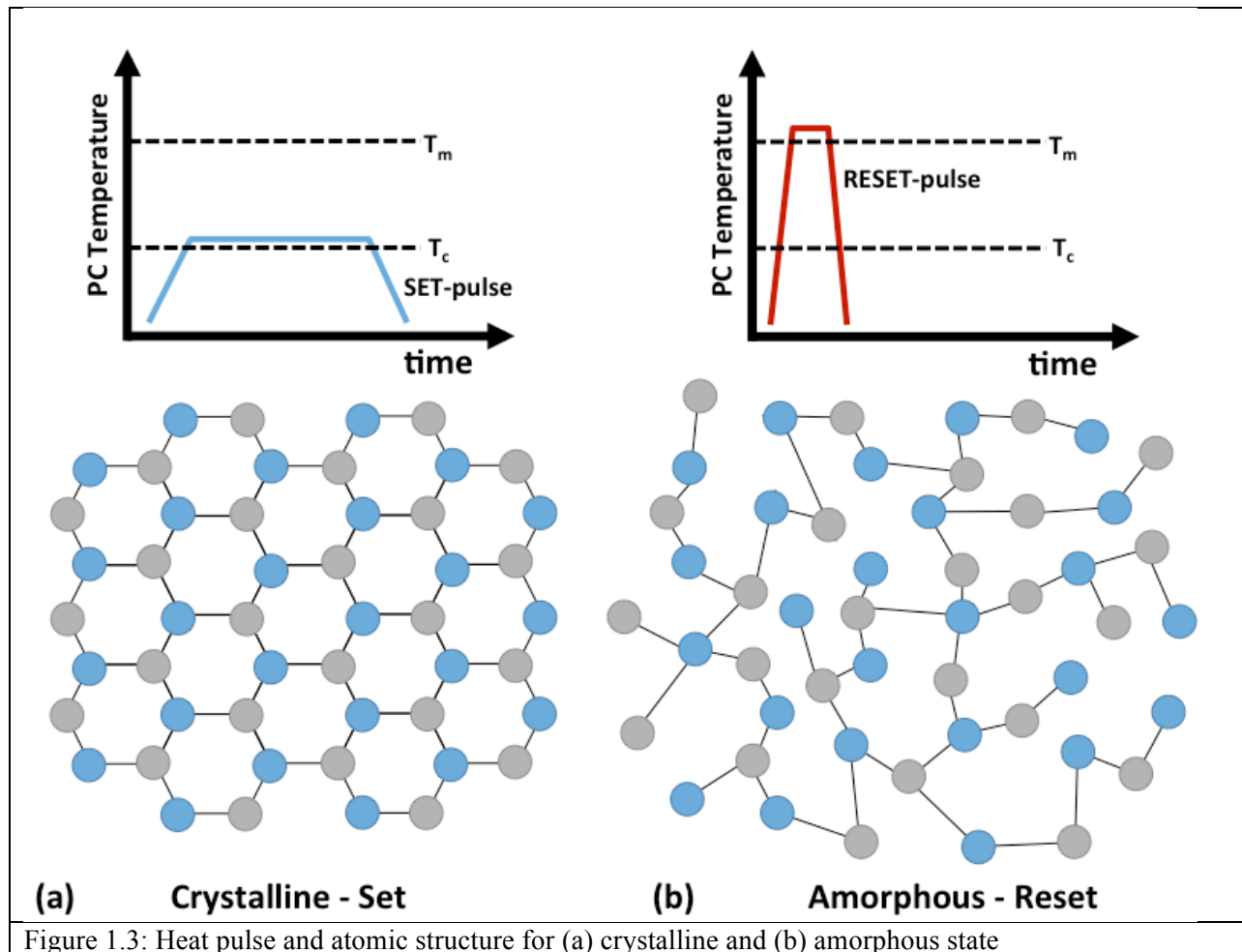
Fig. 1.2 shows the insertion loss and isolation data for SPDT switches using the different RF switch technologies discussed above. The PC RF switch has the lowest insertion loss compared to all switch technologies while still maintaining adequate isolation. Four-terminal RF PC switches show the most promise for integration in reconfigurable RF circuits because they are non-volatile and have a small footprint compared to the other technologies.



1.3 Phase Change History and Physics

In 1968, Ovshinsky first discovered reversible electronic switching from a highly resistive state to a conductive state with the application of an electric field in an evaporated GeAsSiTe thin film [18]. These materials became known as phase change (PC) materials because they consist of an amorphous high resistivity phase and a crystalline low resistivity phase. The PC material is switched between states

through the use of heat pulses. To crystallize the PC material, a heat pulse is applied to raise its temperature above the crystallization temperature long enough to allow for the material to crystallize (fig. 1.3(a)). In order to amorphize the material, a short heat pulse is applied to melt the PC material which is then it is quickly quenched to prevent reordering of the crystal lattice (fig 1.3(b)).

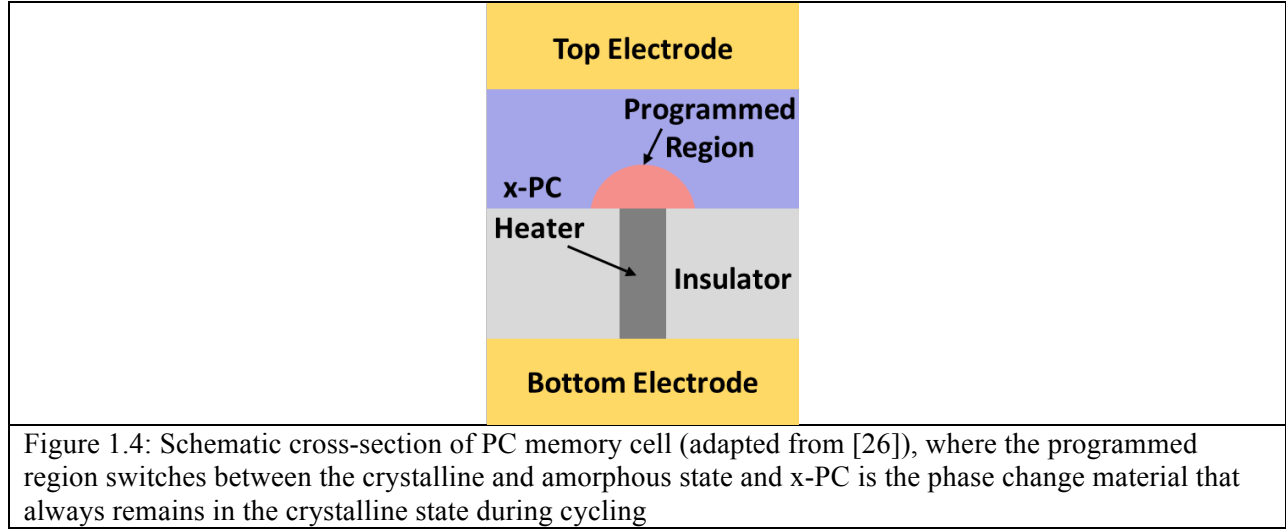


PC materials also have a change in their optical properties that is associated with their shift in phase. In the crystalline phase, the material has high reflectivity, and in the amorphous phase, it has low reflectivity [19]. Optical data storage systems use PC materials in CD-RW and DVD-RW, exploiting the difference in reflectance between the crystalline and amorphous state to store data [19]. A fast, high power laser or current pulse is used to amorphize the phase change material which results in it having a

low reflectivity and high resistivity [20]. A longer, lower power laser or current pulse is used to crystalize the material which results in it having high reflectivity and low resistivity [20].

In 1986, Te-Ge-Sn-Au thin films were demonstrated for use in rewritable disk media [21]. Crystallization of the phase change material was obtained using a 1 μ s, 2 mW laser pulse with the amorphization requiring a 0.2 μ s, 6 mW laser pulse [21]. Laser pulses as short as 120 fs have been used to create amorphous marks in optical media that contains GeSbTe as the PC material for use in RW-DVDs [22].

PC materials have also been used as resistive memory cell, where the resistance of the memory cell in the crystalline state is a “1” and the resistance in the amorphous state is a “0”. Unlike in optical media, the memory cells are not programmed by using laser pulses, but instead by passing current through the PC material and inducing joule heating [19]. When the PC material is in the amorphous phase, threshold switching is needed to allow for enough current to flow in order to cause joule heating and allow for permanent memory switching [19], [23], [24]. To aid in heating of the PC material, a heater is placed in series with the memory cell as seen in fig. 3. The PC material that transforms between the ON (low resistance) and OFF (high resistance) state is mushroom shaped just over the heater (fig. 1.4). This topology is not preferred to be used as an RF switch due to the additional series resistance of the heater. In addition, the RF signal and programming signal share the same path. The resistance of the memory cell in the ON-state is about 2 k Ω due in part to the additional resistance of the heater [25].



Choosing an appropriate PC material for use in an RF switch is critical in determining its performance. Not only is a large R_{OFF}/R_{ON} ratio ($> 10^4$) important but so is the resistivity of the material in the crystalline state. The lower the resistivity of the PC material in the crystalline state, the smaller the switch can be made, resulting in a smaller C_{OFF} and less power required to switch the device. GeSbTe (GST) is a common PC material used in PC memory; however, it only has a crystalline resistivity of $2 \times 10^{-4} \Omega\cdot\text{m}$. On the other hand, GeTe has been reported to have a resistivity that is almost two orders of magnitude lower [27]–[29]. This difference in resistivity results in PC memory cells having a lower ON resistance (30Ω vs. $2 \text{ k}\Omega$ for GST) that can be cycled up to 10^5 times [25]. While this is not as high as GST ($> 10^7$), it still demonstrates preliminary reliability for us as an electronic switch.

1.4 RF Phase Change Switches

1.4.1 Via Style PC Switch

There are three different types of RF PC switch configurations: via style, direct heating and indirect heating. Via style RF switches have been demonstrated many times [3], [4], [17], [29], [30]. They are similar to a PC memory cell without the series heater (fig. 1.5). Via style RF switches are

popular because they are easily to fabricate and can be easily integrated into a backend CMOS process. However, these switches have two main problems: the RF and programming signal share the same path and they are difficult to fully crystalize due to filament formation [24], [29], [31]. The places where the via style switches can be used in RF circuits are limited because the RF and programming signal share the same path. Fig.4 shows the configuration the via style switches used to reconfigure inductors in an LC-VCO [4]. The programming current comes from the middle terminal using microwave (Ground-Signal-Ground) probes (fig. 1.5). In a fully implemented system, these probes would need to be replaced with MEMS probes. The use of transistors instead of probes to transform the PC material (drive current off 100 mA for two switches [29]) would result in at least 100 fF of additional capacitance that would degrade the RF performance of the switch. These switches are difficult to fully crystalize due to filament formation through the amorphous material [29], [31]. As discussed earlier, a threshold switching event must occur first in the amorphous region before enough current is allowed to pass through and cause enough joule heating to occur to crystalize the material [19], [23], [24]. The threshold switching event occurs at the weakest amorphous region and depends on the amorphous region's size and shape [24]. This can lead to the formation of a crystalline firmament thought the amorphous region [24], [29], [31]. However, multiple pulses can be used to fully crystalize the material [3].

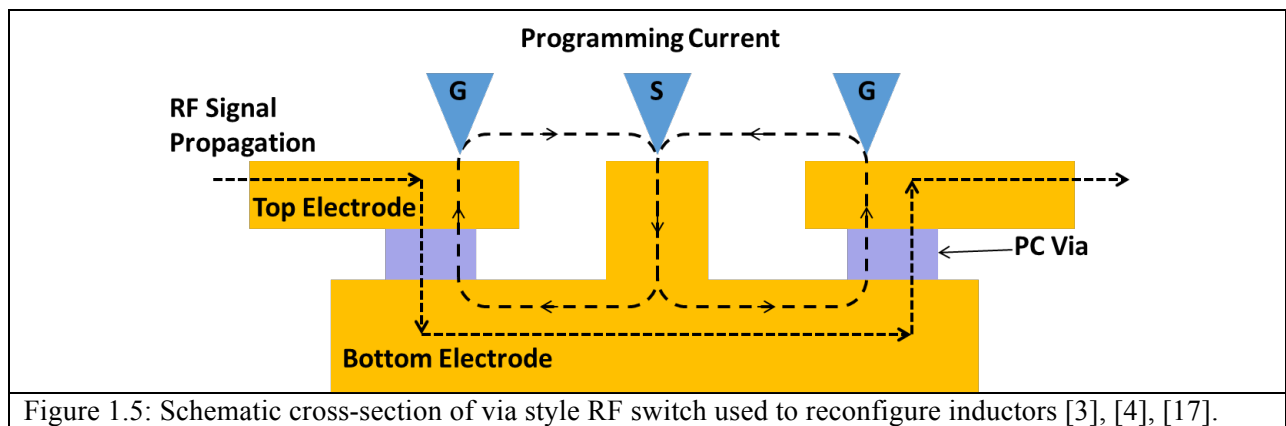


Figure 1.5: Schematic cross-section of via style RF switch used to reconfigure inductors [3], [4], [17].

1.4.2 Direct Heating PC Switch

A heater in direct contact with the PC material can be used to prevent the filament formation and to separate the programming path from the signal path. Carbon nanotubes have been used in direct contact with PC memory cells to reduce programming currents [32]–[34]. A 4-terminal RF switch has been demonstrated to have 0.6 dB of isolation in the ON-state and 20 dB of insertion loss at 20 GHz resulting in a 3.7 THz switch [35]. The device is set up similar to a via style switch except the RF signal propagates horizontally through the device while the programming current travels vertically through the device. This design may still have the issue of filament formation vertically in the device, making it difficult to fully turn on. By placing the heater in direct contact with the phase change, the power required to switch the device is less than 100 mW [35]. The downside to this design is that the heater is still electrically coupled to the RF switch. This results in a shunting of the RF signal to ground through the heater. To mitigate that effect, a high resistance heater must be used. This results in larger programming voltages (16 V) [35].

1.4.3 Indirect Heating PC Switch

The use of indirect heating can solve many of the problems seen in via style and direct heating RF switches. A micro-heater separated by a dielectric barrier layer can be placed above or below the PC material and can be used to switch the device. The use of a 1 μm thick Pt heater on top of a lateral PC memory cell was shown to crystallize the PC material and was separated by a SiO_x/SiN barrier layer [36], [37]. However, the heater had a 10 μs time constant and only reached temperatures up to 270 $^\circ\text{C}$, making it impossible to turn the switch off [36], [37].

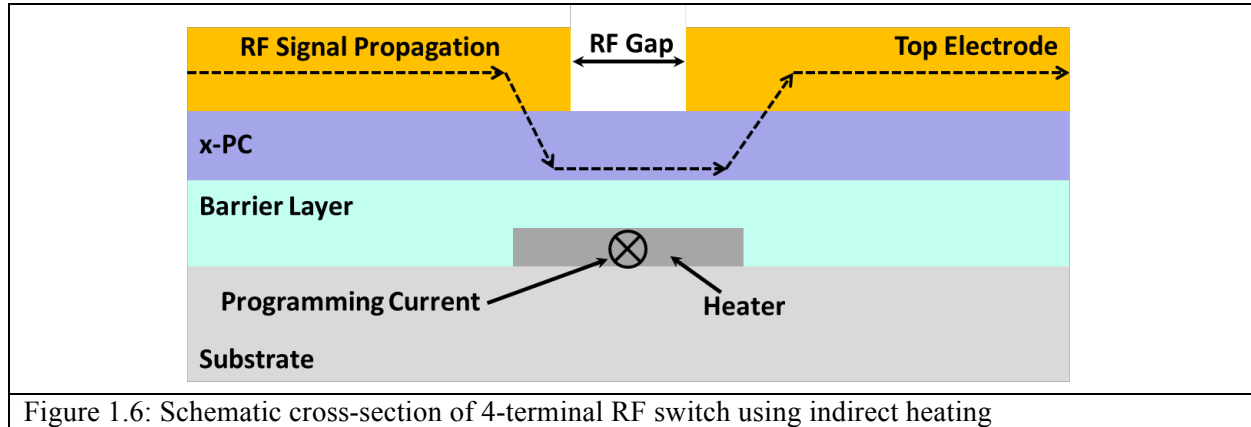
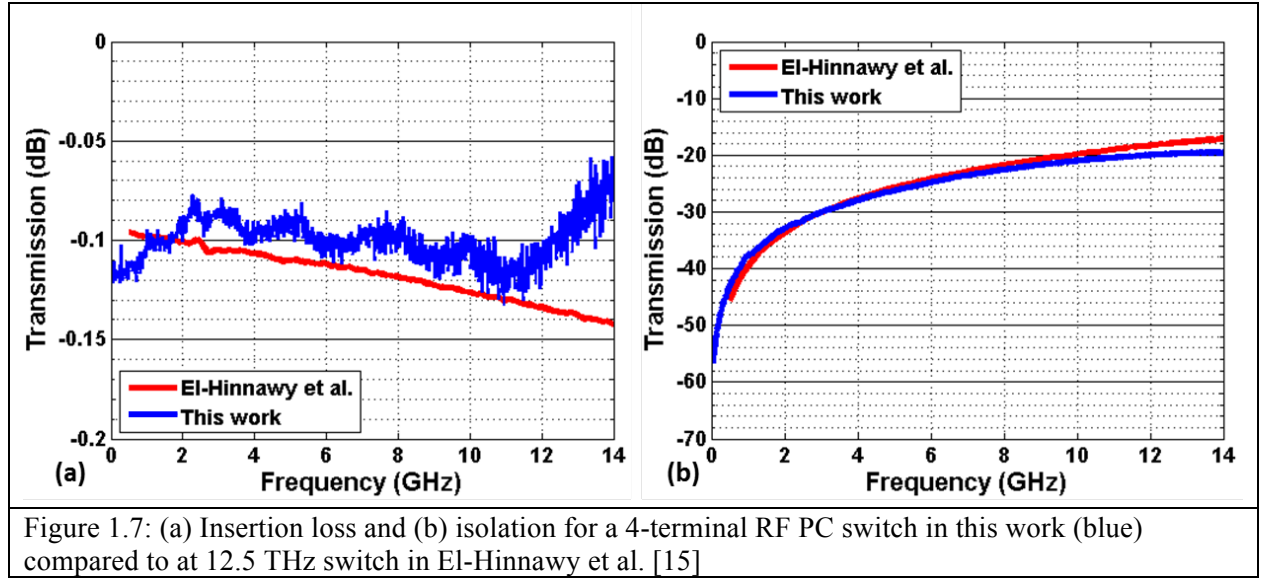


Figure 1.6: Schematic cross-section of 4-terminal RF switch using indirect heating

For an RF switch with an indirect heater, turning the switch off can require up to 4 W of power [38] while less than 100 mW [35] is required for a switch with a direct heater. A micro-heater is separated from a PC layer by an electrically insulating barrier layer (fig. 1.6). The heater is used to transform the PC material between the amorphous and crystalline phases. The RF signal propagates across one electrode down into the PC material and then back up to the other electrode. Enough current must flow through the micro-heater for it to reach temperatures greater than the melting temperature of GeTe (723 °C [39]). The addition of the dielectric barrier layer between the heater and the PC layer results in the heater needing to reach temperatures in excess of 1000 °C to successfully melt the phase change material. This can require power ranging between 0.5 W to 4 W, depending on the pulse length [38]. The cooling time of the system is also important for these switches. To amorphize the PC material, it must first be melted and then quickly quenched below the crystallization temperature (185 – 200 °C [27] [29]). The quench time required for the switch is dependent on the crystallization time of the PC material. It has been reported that the crystallization time for GeTe can be as fast as 16-30 ns [40]–[43] and is very dependent on the stoichiometry of the GeTe [41] [43]. The switches in this thesis were designed to have a cooling time (time from melting temperature to crystallization temperature) of less than 100 ns to ensure they could be amorphized.



The best in class 4-terminal RF switch has reported an F_{CO} of 12.5 THz [15] with an insertion loss of 0.16 dB and an isolation of -15 dB at 20 GHz [15]. This particular switch is 30 μm wide with an RF gap (fig 5) of 0.9 μm [15]. A NiCrSi micro-heater with SiN_x dielectric barrier is used in this switch. This thesis seeks to improve upon this state-of-the-art switch by developing a low resistivity W micro-heater, AlN barrier layer and lower resistivity GeTe and then integrating these components into the switch. Fig. 6 compares the insertion loss and isolation of a 4-terminal RF PC switch from this work to El-Hinnawy et al. [15]. The insertion loss for both switches is similar while the isolation is slightly higher in this work (19.6 dB vs. 17.1 dB at 14 GHz). The switch in this work is only 20 μm wide (vs. 30 μm) and therefore takes less power to switch the device. Therefore, this thesis does make significant advancements to the state-of-the-art RF PC switch.

1.5 Thesis Outline

The rest of the thesis will discuss the details of these switch advancements. Chapter 2 will discuss how to accurately model the thermal response of the switch. It will show the effects of changing the width of the heater, RF gap length and barrier layer thickness as well the use of a notch in the PC layer to reduce the power required to switch the device. Chapter 3 will discuss the process flow used to

fabricate the switch and will detail the improvements made in the heater, barrier layer and PC material. Chapter 4 will show the DC measurement setups used to test the fabricated switches. It will compare R_{on} for different switch layouts and the respective power required for switching. The effect of AlN thickness, RF gap length heater width and switch width will all be examined. Chapter 5 discusses the RF measurement setup as well as the RF performance of the switches measured in Chapter 4. Chapter 6 will show the process used to integrate these switches with RF CMOS circuits to create an LC-VCO and a 3/5 GHz LNA. It will also attempt to differentiate the effect of the solder bump bonding process from the PC switch on the RF performance of the LNA. Finally, Chapter 7 will summarize all the advancements made in this thesis and what further steps can be taken to improve the performance of the switch.

Chapter 2: Phase Change RF Switch Design Considerations and Impact on Efficacy

2.1 Abstract

In this chapter, a 3D model of a 4-terminal inline RF phase change switch is simulated and matched to measurement results. Temperature dependent thermal and electrical properties were included to insure the model's accuracy. Once the accuracy of the model was validated, a less complex 2D model was used to more quickly scan the design space and determine the effect of RF gap length, heater width and barrier layer thickness on minimum power to amorphize (MPA) and cutoff frequency (F_{CO}) of the switch. From the simulation results, the RF gap has the largest impact on RF performance. Reducing the RF gap length from 900 nm to 100 nm increases the F_{CO} from 15 THz to 45 THz with a 50% increase in MPA. This increase in MPA can be mitigated with the use of a notch design. The use of a notch is more efficient in reducing the MPA than increasing the RF gap length. For the same MPA, the notched switch has an F_{CO} of 32 THz while increasing the RF gap results in an F_{CO} of 28 THz.

2.2 Introduction

The ability to model and accurately simulate the electrical and thermal response of the 4-terminal RF PC switch is important in understanding the design limitations of the switch. While fabricating and testing RF switches is the only true way to determine the functionality and performance of a specific switch design, it can be a costly and time consuming processes. An accurate model and the ability quickly simulate many switch designs can be used to provide insight on how the functionality and performance of switch may change when sweeping a design space.

This chapter will discuss the design, modeling and simulation results of a 4-terminal inline RF phase change switch. The basic principles of the switch functionality will be explained followed by an explanation of the properties that were included in the model to ensure accurate results. Simulation results of a 3D model will be compared to the measurement results of a fabricated switch.

There are four design variables that affect the minimum power to amorphize (MPA), heater temperature, cutoff frequency (F_{CO}) and current density in the heater which are: RF gap length, heater width, barrier layer thickness and notch depth. These specific parameters will be defined, analyzed and discussed in detail below. In addition, the effects of increasing amorphization pulse width on MPA, heater temperature and cooling time will be shown.

2.3 RF Phase Change Switch Design

Fig. 2.1(a) shows the basic design of the switch. A thin film resistor which acts as a heater is placed on top of an electrically insulating substrate. A dielectric barrier layer is placed between the heater and the PC material. Metal electrodes on top of the PC material are then used to define the switch. The length of the RF gap is the main determining factor of the switch resistance in the ON-state. In the ON-state (fig. 2.1(b)), the RF signal propagates through the top electrode down into the crystalline PC-material then back up to the top electrode. In the OFF-state (fig. 2.1(c)), the RF signal propagates through the top electrode, then hits the amorphous PC-material and reflects back. The heater is used to transform the switch between the two states. The heat generated in the heater must flow across the barrier layer to raise the temperature of the PC-material. The presence of the barrier layer does result in an inefficient heating of the PC-material but is necessary in order to separate the RF signal path from the programming path.

By forcing current through the heater, the PC-material in the RF-gap can be heated allowing for transformation between the crystalline ON-state and the amorphous OFF-state. The heating profiles are shown in 2.1(d), where a wide pulse (blue) is used to raise the temperature of the PC-material above the

crystallization temperature and is then held there long enough to completely crystallize the material in the RF gap. A narrow pulse (red) is used to quickly raise the temperature of the PC-material in the RF gap above the melting temperature and which is then quickly quenched to ensure the PC-material is in the amorphous state. The effect of the OFF-pulse width will be discussed later in the chapter.

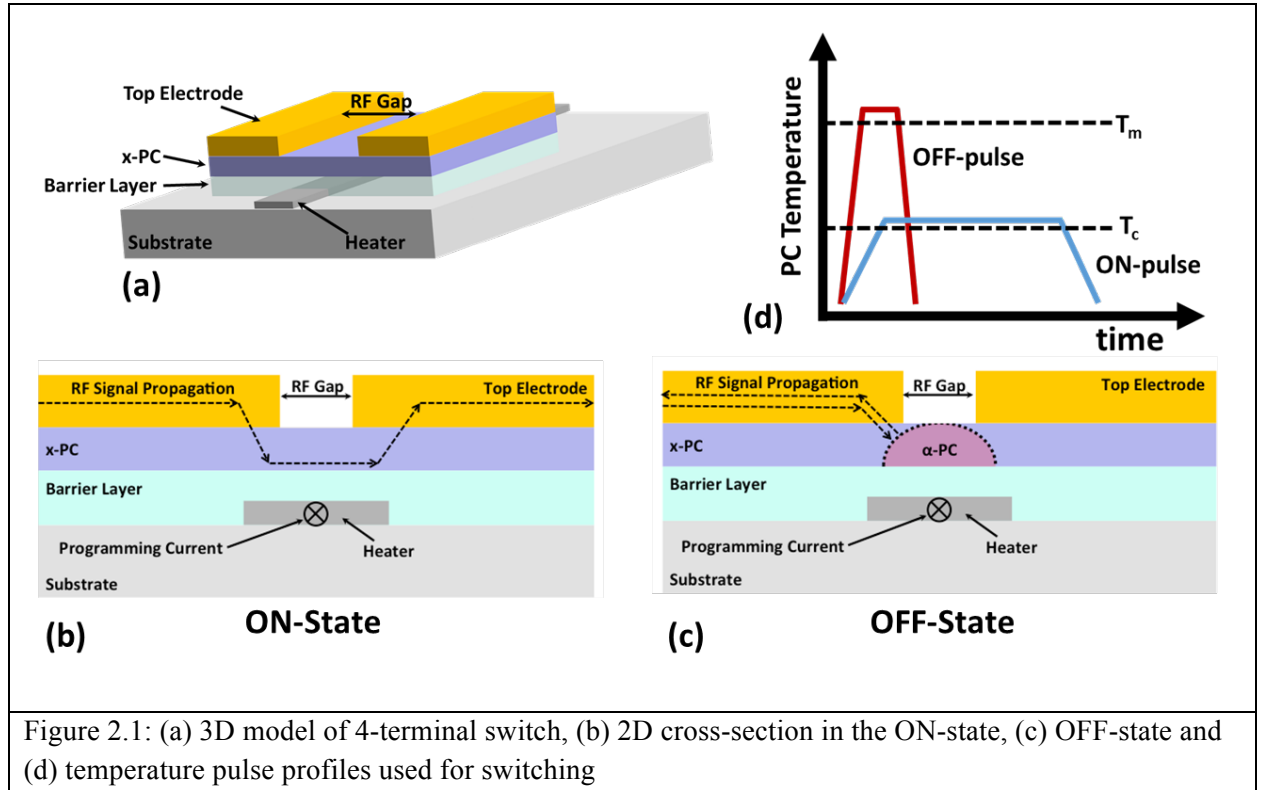
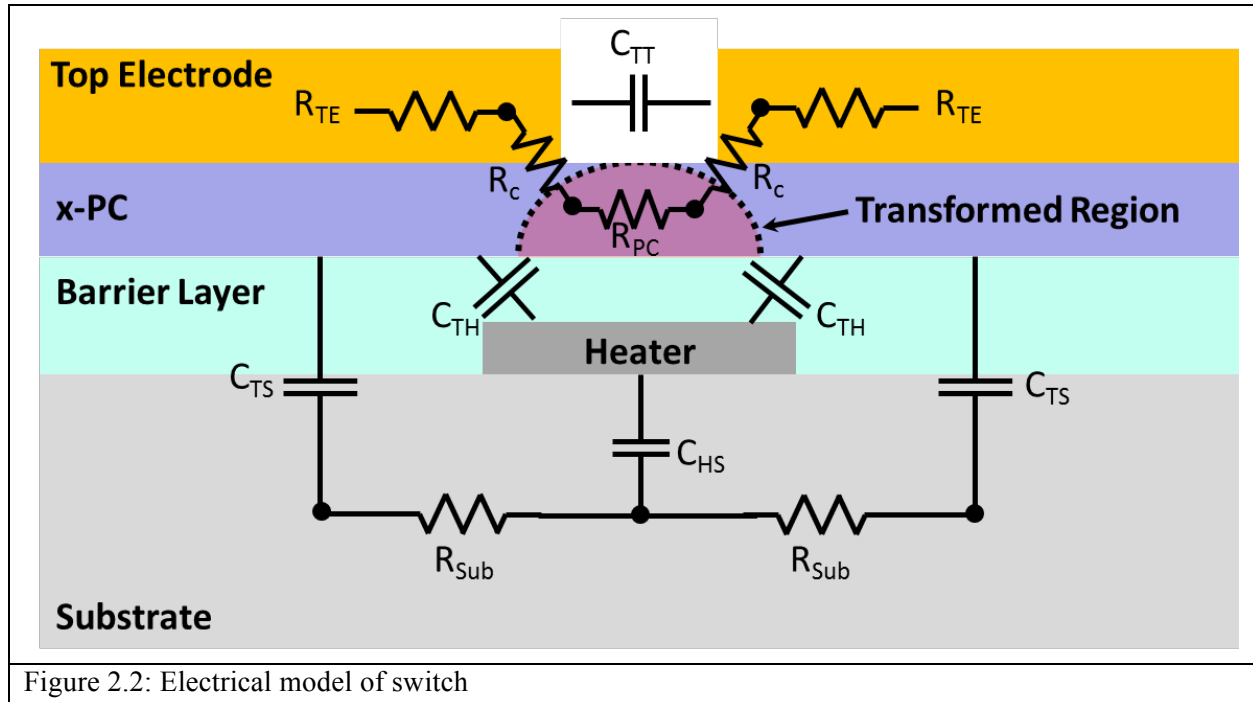


Figure 2.1: (a) 3D model of 4-terminal switch, (b) 2D cross-section in the ON-state, (c) OFF-state and (d) temperature pulse profiles used for switching

The material choices for the barrier layer and the PC-material are most critical in order to maximize the performance of the switch. The resistivity of the PC-material most directly contributes to the ON-state resistance of the switch while the dielectric constant of the barrier layer most directly contributes to the OFF-state capacitance. In the electrical model of the switch (fig. 2.2), the resistance of the switch is comprised of 3 parts: the top electrodes (R_{TE}), the contact resistance between the switch and the PC-material (R_c) and the resistance of the PC-material in the RF-gap (R_{PC}). The non-transformed material is in the crystalline state to assure the lowest ON-state resistance possible. Because the top electrode is a highly conductive metal such as Au, R_{TE} has a minimal contribution to the total resistance of

switch. By choosing a proper contact metal and maintaining a pristine interface between the top electrode and PC-material, R_c can also be minimized which leads to R_{PC} being the largest contributor to the resistance of the PC switch.

Choosing an appropriate material for the PC layer is also critical. GST is a common PC-material used in phase change memory (PCM) but has a resistivity of $5 \times 10^{-4} \Omega\text{-m}$ [25]; however, GeTe has a resistivity that is over two orders of magnitude lower than GST of $3\text{-}4 \times 10^{-6} \Omega\text{-m}$ [25], [29], [44], and is shown to be more suitable in RF PC-switch applications [29], [44]. A resistivity as low as $1.5 \times 10^{-6} \Omega\text{-m}$ for GeTe films has been achieved in this work and will be discussed in more detail in a later chapter.



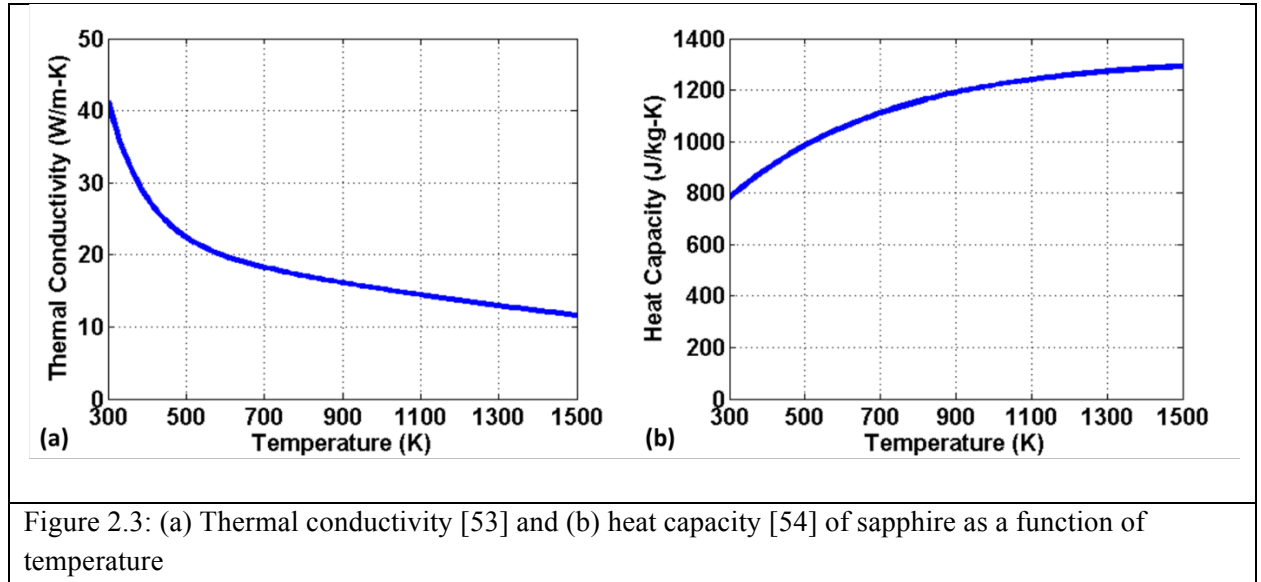
The capacitance of the switch in the OFF-state is comprised from 3 main sources: the capacitance between the traces and heater to the substrate (C_{TS} , C_{HS}), the capacitance between the two traces (C_{TT}) and the capacitance between the trace and the heater (C_{TH}). By choosing an electrically insulating substrate such as sapphire, R_{Sub} is large and thereby minimizes the contributions of C_{TS} and C_{TH} to the overall OFF-state capacitance of the switch. C_{TT} is determined by the RF gap length with a longer

RF gap resulting in a lower C_{TT} ; however, this is at the expense of R_{PC} and is therefore difficult to reduce. The capacitance between the heater and the traces C_{TH} is a function of the heater width as well as the thickness and dielectric constant of the barrier layer. The size effect of the heater will be discussed later in the chapter. The choice of dielectric material for the barrier layer is not as simple as choosing one with the lowest dielectric constant to minimize C_{TH} , because not only does the barrier layer have to electrically isolate the heater from the RF signal path but it also must allow heat to flow from the heater to the PC-material. Therefore, the thermal conductivity (k_{th}) of the barrier layer must also be considered. In previous examples of 4-terminal RF phase change switches [15], [16], [38], SiN_x is used as the barrier layer which has a relative dielectric constant of 7 [45]. The thermal conductivity of a 160 nm of SiN_x film, provided by El-Hinnawy of Northrop Grumman Electronic Systems, was measured to be 1.1 W/m-K using the frequency domain thermal reflectance (FDTR) technique [46]. Using a material with such a low k_{th} will result in a large temperature gradient across the barrier layer thereby limiting heat flow to the PC-material. Using a dielectric with a higher k_{th} , such as AlN, will limit the thermal gradients across the barrier layer and may even allow the thickness of this layer to be increased far beyond what would be achievable using SiN_x . AlN has a slightly higher dielectric constant of 8.0-9.2 [47], but has a bulk k_{th} of 285 W/m-K [48]. The k_{th} for sputtered AlN films has been measured to be as high as 130 W/m-K [49]. In the model that is simulated, a more modest value of 50 W/m-K is arbitrarily used and the simulation results are relatively insensitive for values above 10 w/m-K.

2.4 Model Setup

A 3D model of the 4-terminal inline RF phase change switch was built and simulated using COMSOL Multiphysics software. In order to simulate the thermal response of the switch, three physics modules including heat transfer, electric currents and electric circuits were used concurrently and were coupled to each other. The material properties required for the simulation were heat capacity (C_p), density (ρ), thermal conductivity (k_{th}), relative permittivity (ϵ_r), resistivity at 300 K (ρ_{300}) and temperature coefficient of resistivity (α). Some of these values were measured while others were taken

from literature. There are a few main parameters that must be included in the model to ensure its accuracy. The measured resistivity and TCR of the W heater are required to ensure proper power dissipation during the voltage pulse across the heater. The temperature dependence of sapphire's k_{th} (fig. 2.3(a)) and C_p (fig. 2.3(b)) is needed for the heater to reach the required temperature necessary to melt the PC-material. A thermal interface layer between the W heater and sapphire substrate is also necessary for the heater to reach the desired temperature. A thermal conductance of $200 \text{ MW/m}^2\text{-K}$ is used for this interface and is based on the thermal conductance of Cu and Al with sapphire, $200\text{-}300 \text{ MW/m}^2\text{-K}$ [50] and $90 \text{ MW/m}^2\text{-K}$ [51], respectively. These two metals are chosen because their Debye temperatures (Cu – 343.5 K, Al – 428 K) are the closest match to W Debye temperature (400 K) [52].



A thermal interface layer of $200 \text{ MW/m}^2\text{-K}$ was also used between the AlN and sapphire; however, this did not significantly change the results. The thermal interface was kept in the model because it is known to exist despite not playing a significant factor simulation results. Temperature thermal conductivities for W and Au were also added and were based on the Wiedemann-Franz law [52] (eq. 2.1). The thermal conductivity at temperature (k_{th-T}) is shown in eq. 2.1, where k_{th-300} and ρ_{300} are

thermal conductivity and resistivity of the metal at room temperature, respectively. However, this does not significantly effect to outcome of the simulation.

$$k_{th-T} = \frac{k_{th-300} \times \rho_{300}}{\rho_{300}(1 + \alpha \Delta T)} \quad (2.1)$$

The material properties used for the model are shown in table 2.1. Because the fabricated devices are pulsed using a pulse generator with a 50 Ω source impedance, the same set up must be modeled using the electric circuits module (fig. 2.4). This is necessary to make the appropriate correction for the reflected voltage due to the heater resistance not matching the source impedance of the pulse generator during the entire duration of the pulse. The pulse generator output is twice the applied voltage (V_{App}) with a 50 Ω source impedance in an attempt to deliver V_{App} to a 50 Ω load which, in this case, is the heater. However, the heater acts as a variable resistor and its resistance increases as it heats up. This results in an increasing voltage across the heater.

Material	Density (kg/m ³)	C _p (J/kg-K)	k _{th} (W/m-K)	ϵ_r	Resistivity (Ω -m)	TCR
Sapphire	3965	fig. 2.3(b)	fig. 2.3(a)	8.9 \perp c, 11.11 \parallel c [55]	10 ⁶	0
W	19350	132	$\frac{174 \times 7.2^{-8}}{7.2^{-8}(1 + .003(T - 300))}$	1	7.20 ⁻⁸	0.003
AlN	3260	740	50	9 [47]	10 ⁶	0
x-GeTe	6140	303	1	18	1.68 ⁻⁶	0.004
a-GeTe	6140	303	1	18	10	0
Au	19300	129	$\frac{317 \times 3.42^{-8}}{3.42^{-8}(1 + .0024(T - 300))}$	1	3.42 ⁻⁸	0.002
Cu	8960	384	200	1	3.35 ⁻⁸	0.002
SiO ₂	2200	730	1	3.9	10 ⁶	0

Table 2.1: Material properties for use in the model

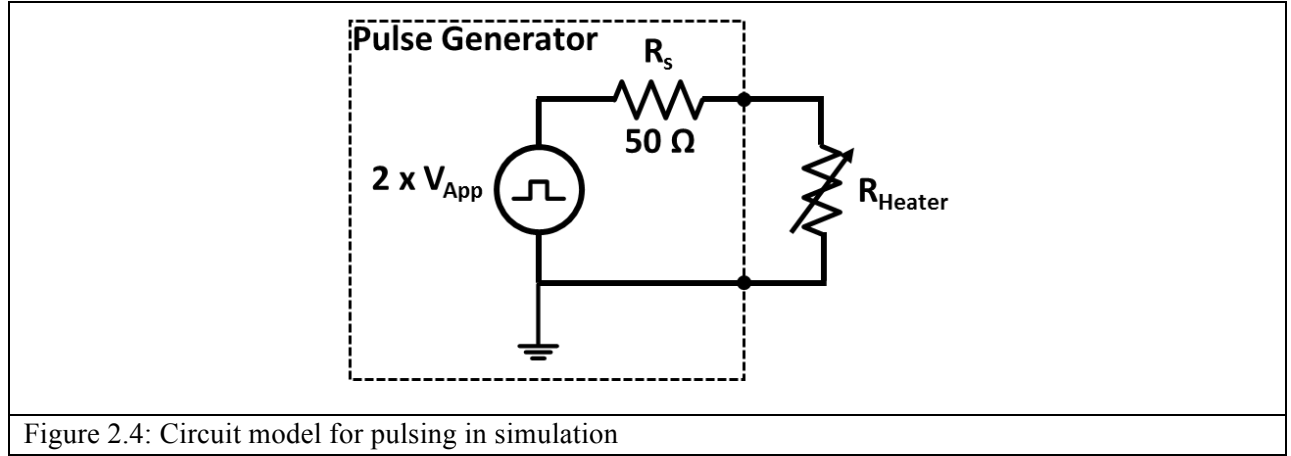


Figure 2.4: Circuit model for pulsing in simulation

To check the validity of the model parameters, the results of experimental measurements on a fabricated switch (fig. 2.5) were compared to simulations. One hundred nanosecond long amorphization pulses with increasing V_{App} were applied across the heater (vertical structure in fig. 2.5(a)) while measuring the switch resistance between RF-In and RF-Out (fig. 2.5(a)). The schematic of the cross-section of the device (fig. 2.5(b)) shows the layer thicknesses, width of the heater and length of the RF gap measured from the FIB cross-section of the device (fig. 2.5(c)). The switch is $20 \mu\text{m}$ wide with a 550 nm long RF gap. The heater is $1.06 \mu\text{m}$ wide and $25 \mu\text{m}$ long with 105 nm of AlN between the heater and the GeTe.

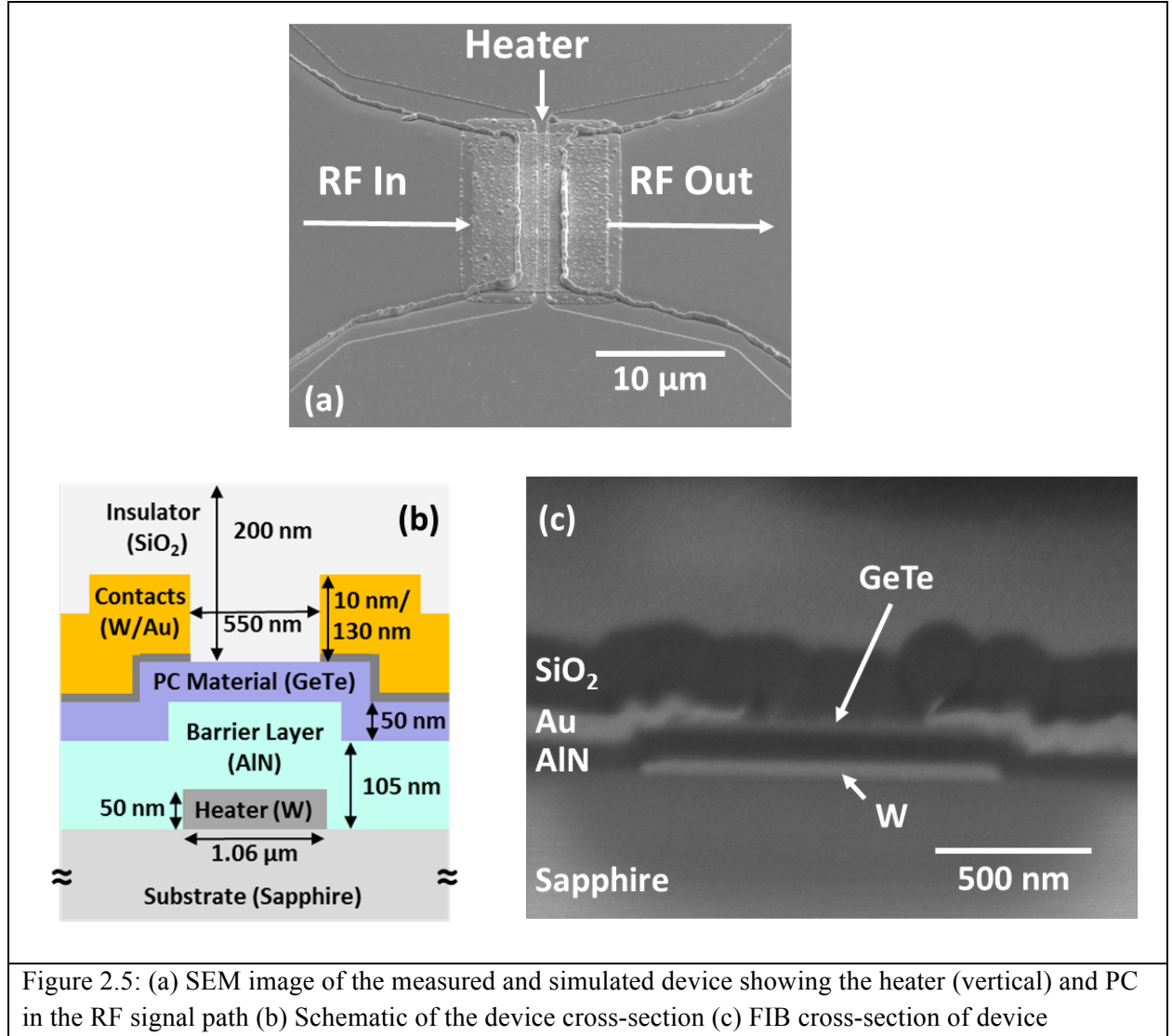


Figure 2.5: (a) SEM image of the measured and simulated device showing the heater (vertical) and PC in the RF signal path (b) Schematic of the device cross-section (c) FIB cross-section of device

2.5 Simulations of 3D Model vs. Measurement Results

Fig 2.6(a) shows the measured switch resistance (blue) after subsequent 100 ns long pulses with increasing pulse power. When V_{App} reaches 8.7V (1.47 W applied pulse power), the resistance of the switch is 50 k Ω and is considered “off”. The simulated temperature (red) at the top of the GeTe in the RF gap increases with applied pulse power and crosses over the melting temperature of the GeTe (996 K [39]) at 1.47 W, resulting in the amorphization of the GeTe. This shows that the measured minimum power to amorphize (MPA) the switch occurs when the top of the GeTe gets slightly above the melting temperature. The 1.47 W is the initial applied power based on the V_{App} and the resistance of the switch at

room temperature. The heater resistance is $39.9\ \Omega$ at room temperature but, as the temperature of the heater rises, the resistance increases to $120\ \Omega$. Therefore, the power being delivered to the heater is decreasing once its resistance is above $50\ \Omega$.

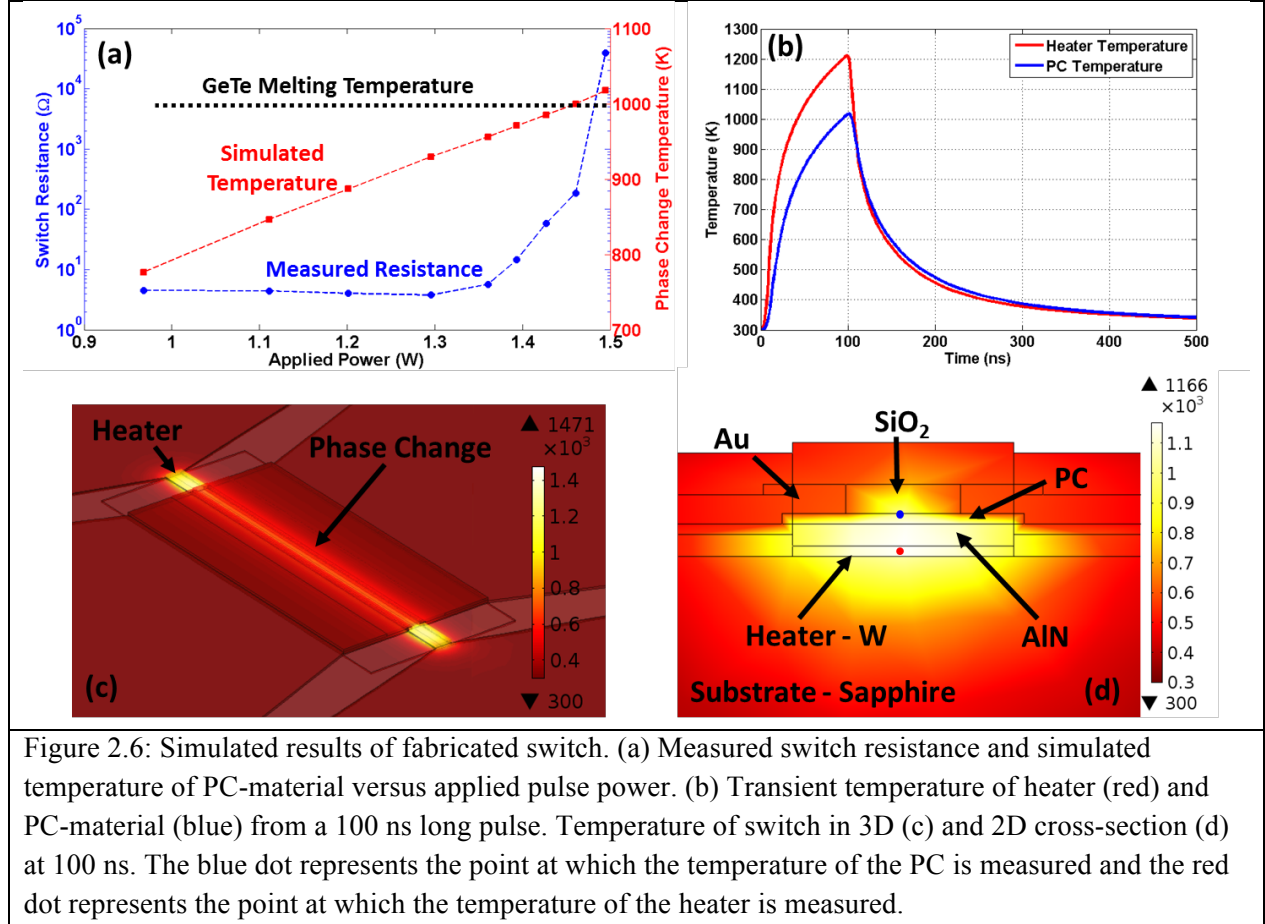


Fig 2.6(b) shows the simulated temperature transient of the MPA pulse for the middle of the heater (red) and the top PC-material (blue) from a 100 ns long pulse. The PC gets slightly above 1000 K by the end of the pulse, while the heater gets slightly above 1200 K. The time it takes for the PC to move from the melting temperature (996 K) to the crystallization temperature (200 K [29]) is less than 100 ns and is fast enough to amorphize the GeTe. The temperature of the switch at 100 ns for the MPA pulse is shown in 3D (fig. 2.6(c)) and 2D cross section (fig. 2.6(d)). Fig. 2.6(c) shows that the maximum temperature of the switch is actually at both ends of the heater where neither PC nor Au is present. The

2D cross-section (2.6(d)) shows the locations where the heater (red point) and PC (blue) temperatures are measured. It should be noted that there is almost zero temperature gradient across the thickness of the AlN barrier layer and that almost all of the temperature difference between the heater and the top of the PC is in the PC layer.

2.6 3D Model vs. 2D Model

Full 3D simulations are time consuming (> 1 hour per transient simulation) and require a significant amount of computing power. For the rest of the simulations in this chapter, 2D models using a cross-section of the device will be simulated (< 5 minutes per transient simulation). Because it is a 2D model, only the heat transfer physics can be used. The heater is set as the heat source in the simulation. The power, P_H , dissipated in the heater is a function of the voltage across the heater and the temperature dependent heater resistance (as shown in eq 2.2), where V_{App} is the voltage from the pulse generator and Γ is the reflection coefficient due to the mismatch between the source and load (R_H) impedance. R_H is the temperature dependent resistance of the heater (as shown in eq 2.3).

$$P_H = \frac{(V_{App}(1+\Gamma))^2}{R_H} \quad (2.2)$$

$$R_H = R_{H0}(1 + \alpha(\bar{T} - 300)) \quad (2.3)$$

R_{H0} is the initial resistance of the heater based on its width, length (25 μm), thickness (50 nm) and the resistivity of the W. \bar{T} is the average temperature of the heater in kelvin and α is the measured TCR of W. R_H is also used to calculate Γ (as shown in eq. 2.4). R_S is the source impedance of the pulse generator (50 Ω) and R_{HC} is the resistance of the heater leads and is estimated to be 6 Ω . The average temperature of heater, \bar{T} , is used to calculate the R_H , because this is the only way it can be implemented in the model. Calculating the average resistance of the heater based on the temperature at each point in the heater is not

possible using a 2D model. The uses of \bar{T} is shown to be an adequate approximation due to its match to the 3D model.

$$\Gamma = \frac{R_H - (R_S + R_{HC})}{R_H + R_S + R_{HC}} \quad (2.4)$$

A 2D model of the switch in fig 2.5 was simulated with the same V_{App} of 8.7 V for a 100 ns long pulse and compared to the 3D simulation (fig. 2.7). The heater reaches nearly the same temperature (center point) for both the 3D and 2D simulations while the PC temperature is about 30 K higher in 2D than in 3D. This difference is most likely a result of the out of plane heat flow that is missing in the 2D simulation. The cooling times for both simulations are identical and the 2D simulation is accurate enough to be used for the remaining simulations in this chapter. The following simulations are intended to demonstrate the effects of adjusting the following variables: RF gap length, heater width, barrier layer thickness, use of a notch in the PC-material and amorphization pulse length. They are not intended to predict the outcome of a specific fabricated switch.

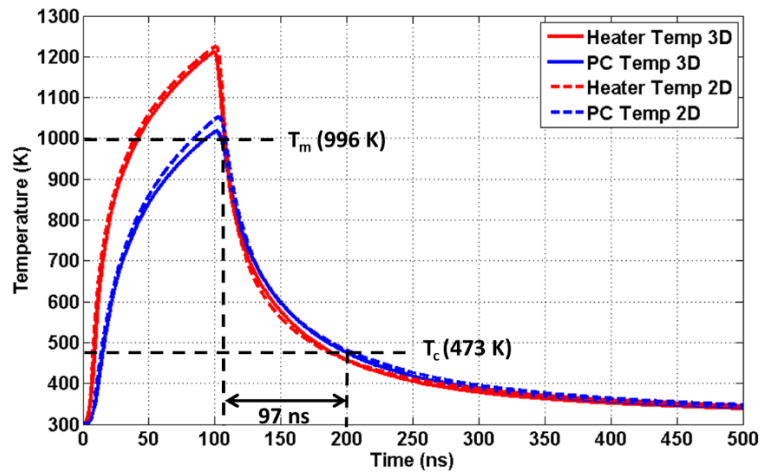
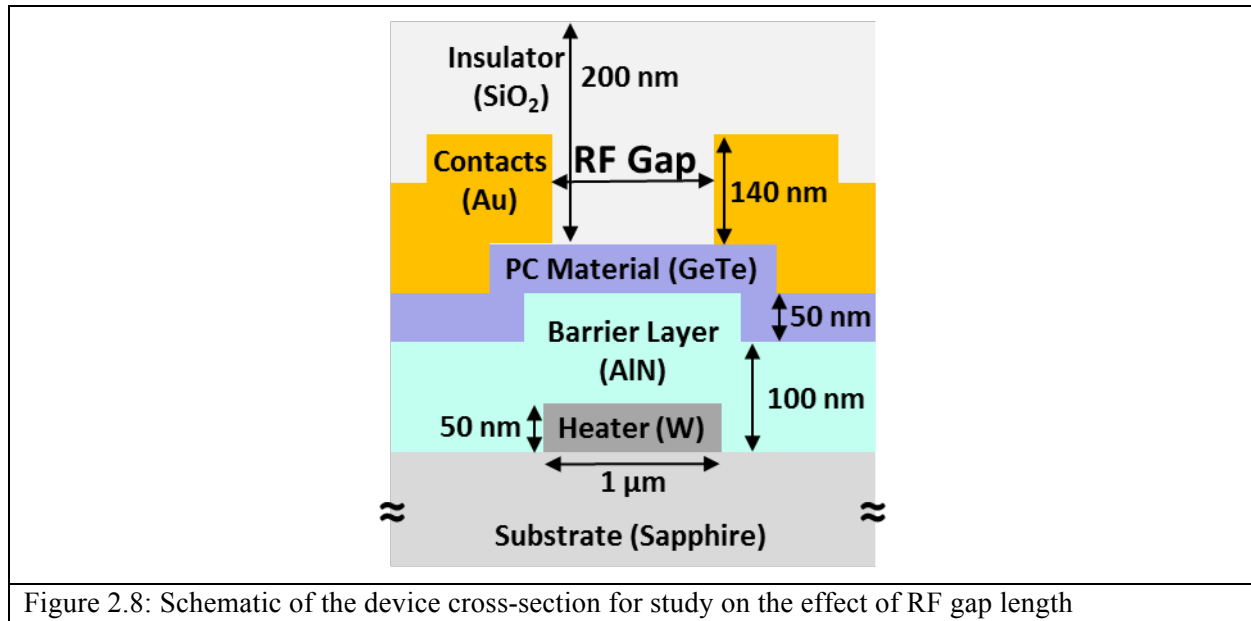


Figure 2.7: Transient temperature of the heater (red) and PC-material (blue) from a 100 ns pulse for both 3D (solid) and 2D (dashed) simulations

2.7 Simulation Results of Design Parameter Sweep

2.7.1 RF Gap Length

The RF gap is the distance between the two electrodes on top of the PC-material (fig 2.8). As previously discussed, the length of this gap most directly contributes to the ON-state resistance of the switch. However, the top electrodes are made from Au and are thermally conductive, thereby creating a shunt path to thermal ground. This shunt path becomes smaller as the RF gap shrinks, making it difficult to melt the PC-material in the gap. A 2D model (fig. 2.8) was simulated while changing the RF gap length from 100 nm to 900 nm long using 100 nm increments. The MPA was found by increasing applied pulse power until the top of the PC-material in the RF gap reached the melting temperature (996 K) by the end of a 100 ns long amorphization pulse.

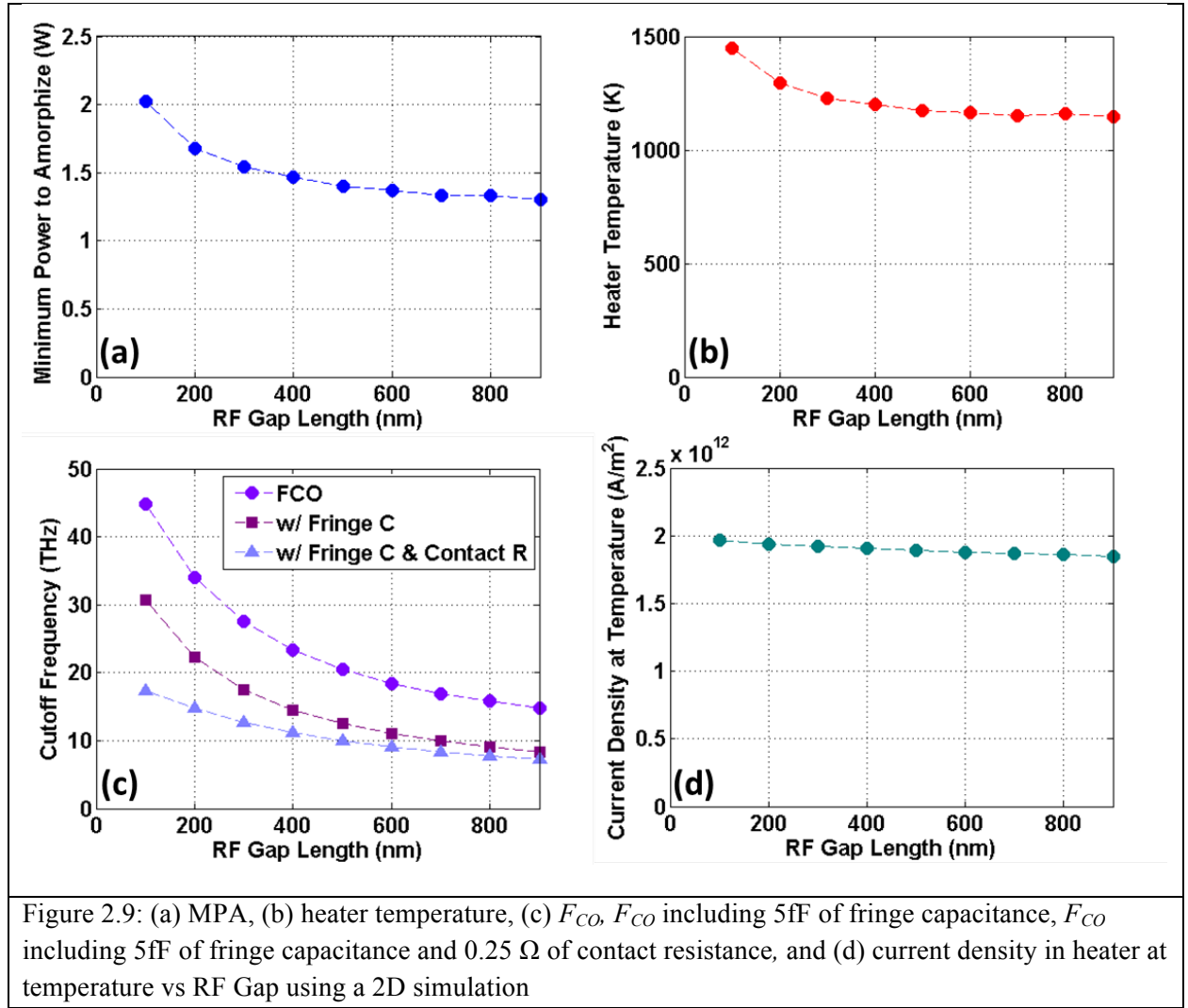


As expected, the MPA of the device decreases with increasing RF gap length (fig. 2.9(a)). However, the trend is not linear. Increasing the length past 500 nm does not decrease the MPA significantly. The temperature of the heater at the end of the 100 ns long MPA pulse (fig. 2.9(b)) also decreases as the RF gap length increases and flattens out at about 1200 K. These two results show that

when the RF gap is small, the top electrodes create larger thermal gradients in the PC-material thereby requiring more power to be generated in the heater to melt the top of the PC-material. However, there will always be a 200 K difference between the heater temperature and the top of the PC because of the thermal gradients present in PC layer.

The F_{CO} (fig. 2.9(c)(circles)) decreases with increasing gap length due to the increase in ON-state resistance (R_{ON}). The OFF-state capacitance (C_{OFF}) decreases slightly with increasing gap length, but the increase in R_{ON} dominates the F_{CO} . The 2D-simulation does not take into account any fringing capacitance that may be present between the pads. When 5 fF of fringing capacitance is added (squares), the F_{CO} decreases by over 14 THz for a 100 nm gap. When 0.25 Ω of contact resistance is also included with the fringing capacitance (triangles), the F_{CO} decreases even more dramatically at shorter RF gaps. These assumptions for fringing capacitance and contact resistances are based on measured results from fabricated devices and will be discussed in the later chapters.

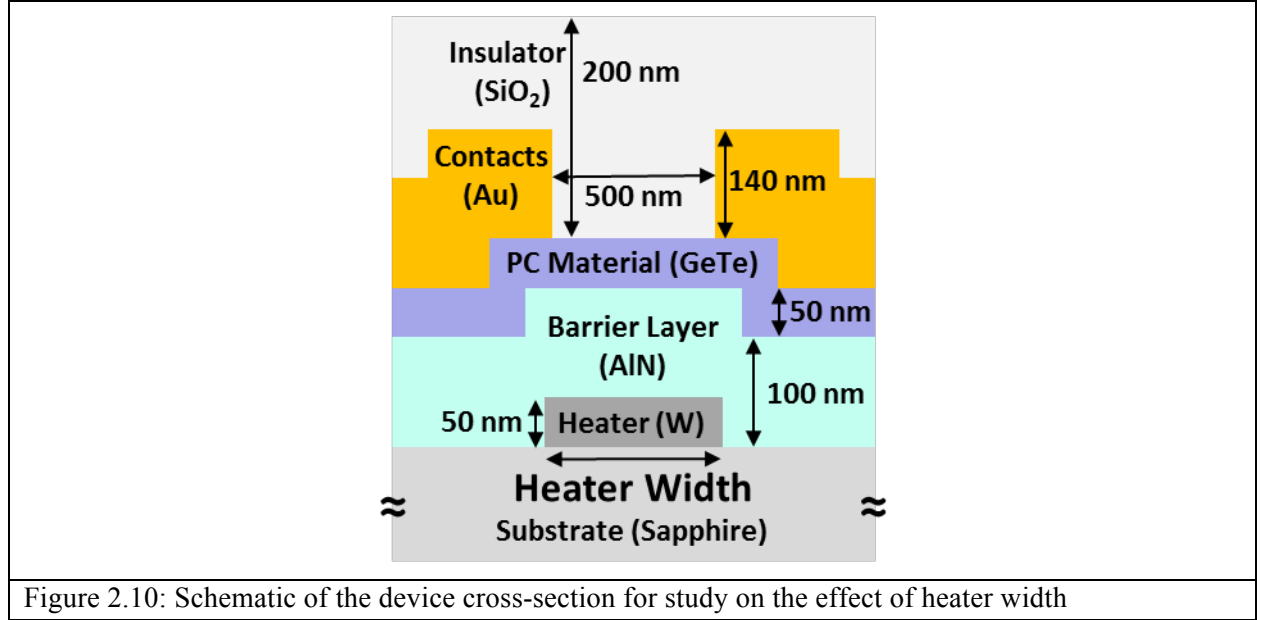
The current density in the heater at 100 ns from the MPA pulse (fig. 2.9(c)) is not significantly affected by RF gap length and reduces by less than 10% when gap length is increased from 100 nm to 900 nm. Minimizing the heater temperature and current density can prolong the lifetime of the heater if electromigration is one of the heater's failure mechanisms [56].



2.7.2 Heater Width

A 2D model was built to simulate the effect of changes in heater width (fig 2.10) while the RF gap length was held constant at 500 nm. A 50 nm thick heater was used on a sapphire substrate with a 100 nm thick AlN barrier layer and 50 nm of GeTe. The MPA (fig. 2.11(a)) increased with heater width. Due to the increase in contact area between the heater and substrate, an increase in power is needed to reach the target temperature because the thermal resistance to ground decreased. As expected, the temperature of the heater remains constant at MPA (fig. 2.11(b)) and, therefore, no additional thermal

gradients are present in the PC-material due to an increase in heater width. The results in fig 2.11(a) suggest that even heaters with sub-micron widths would still require 1.4 W to amorphize the PC-material. The MPA increases at 0.45 W per micron of heater width.



The F_{CO} decreases with increasing heater width (fig. 2.11(c)) from 20 THz at 1 μm to 10 THz at 3 μm . The decrease in F_{CO} is a result of increasing C_{OFF} as R_{ON} remains constant with changes in heater width. The increase in C_{TH} (fig. 2.2) is due to the increase in overlap area between the heater and the top electrode. As expected, the F_{CO} with 5 fF of fringe capacitance and 0.25 Ω of contact resistance becomes less dependent on heater width.

The current density in the heater at temperature decreases with heater width (fig. 2.11(d)); however, after 2 μm the decrease is not significant. Increasing the heater width does not improve performance in any way. The only reason to increase the width of the heater is to reduce the current density if the durability of the heater is in question. However, there are more efficient ways to improve the heater durability than by making the heater wider, such as using switches in parallel to make the heater shorter in length.

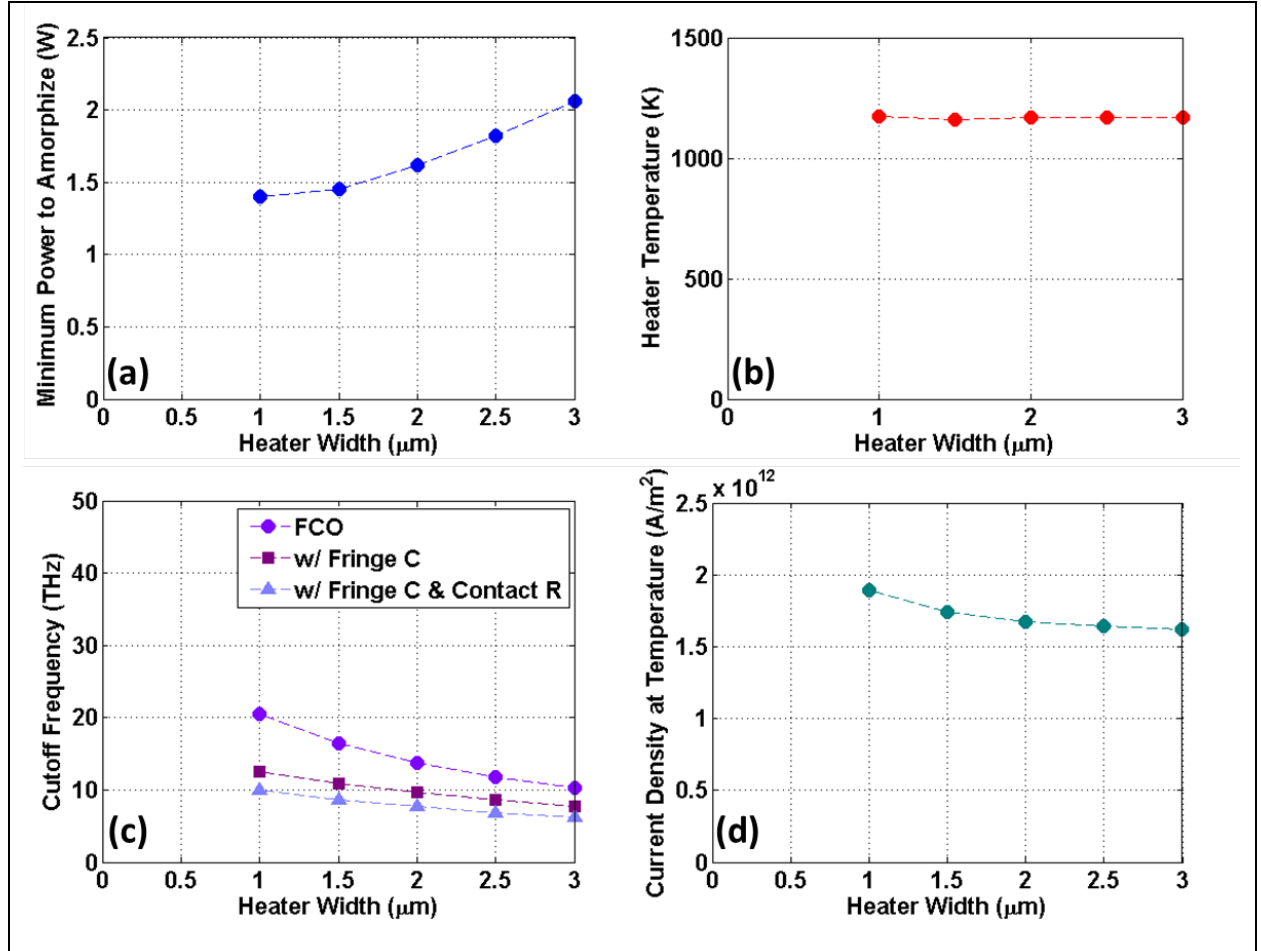
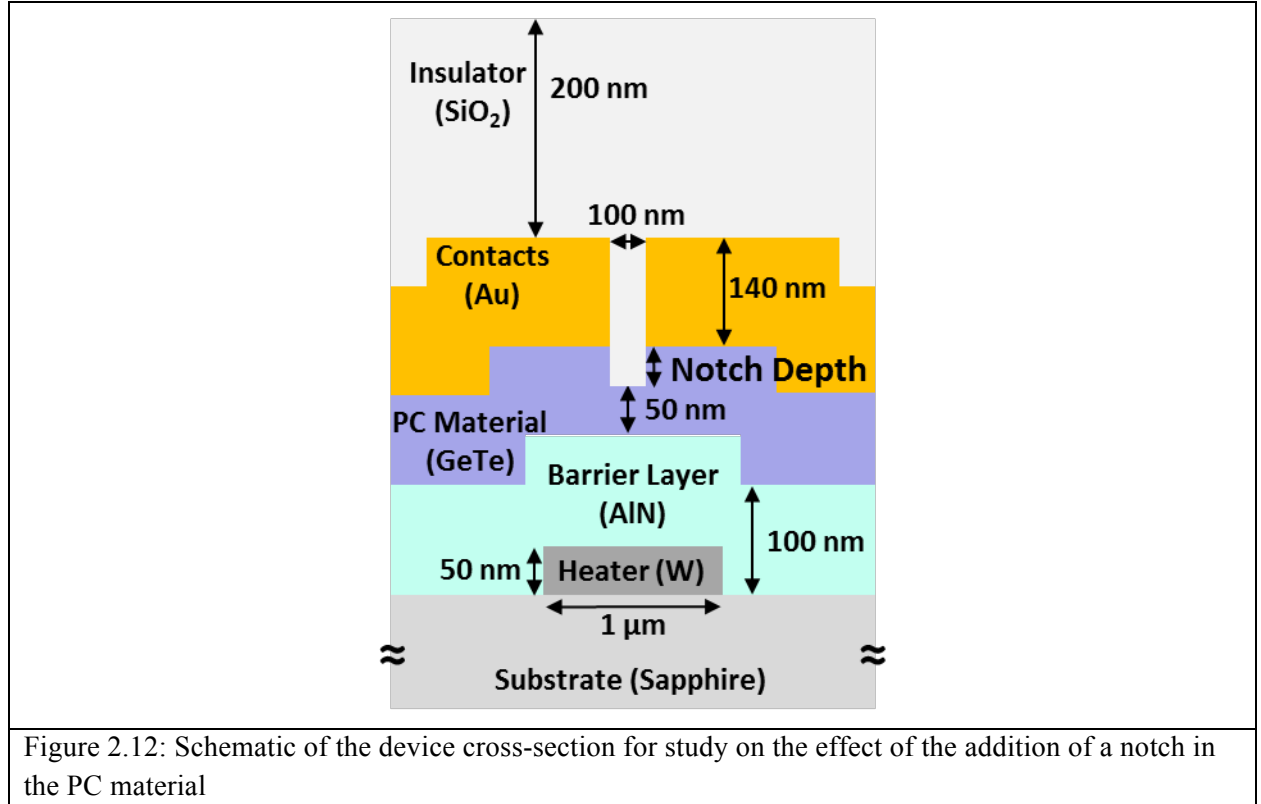


Figure 2.11: (a) MPA, (b) heater temperature, (c) F_{CO} , F_{CO} including 5fF of fringe capacitance, F_{CO} including 5fF of fringe capacitance and 0.25 Ω of contact resistance, and (d) current density in heater at temperature vs RF Gap using a 2D simulation

2.7.3 Notch Design

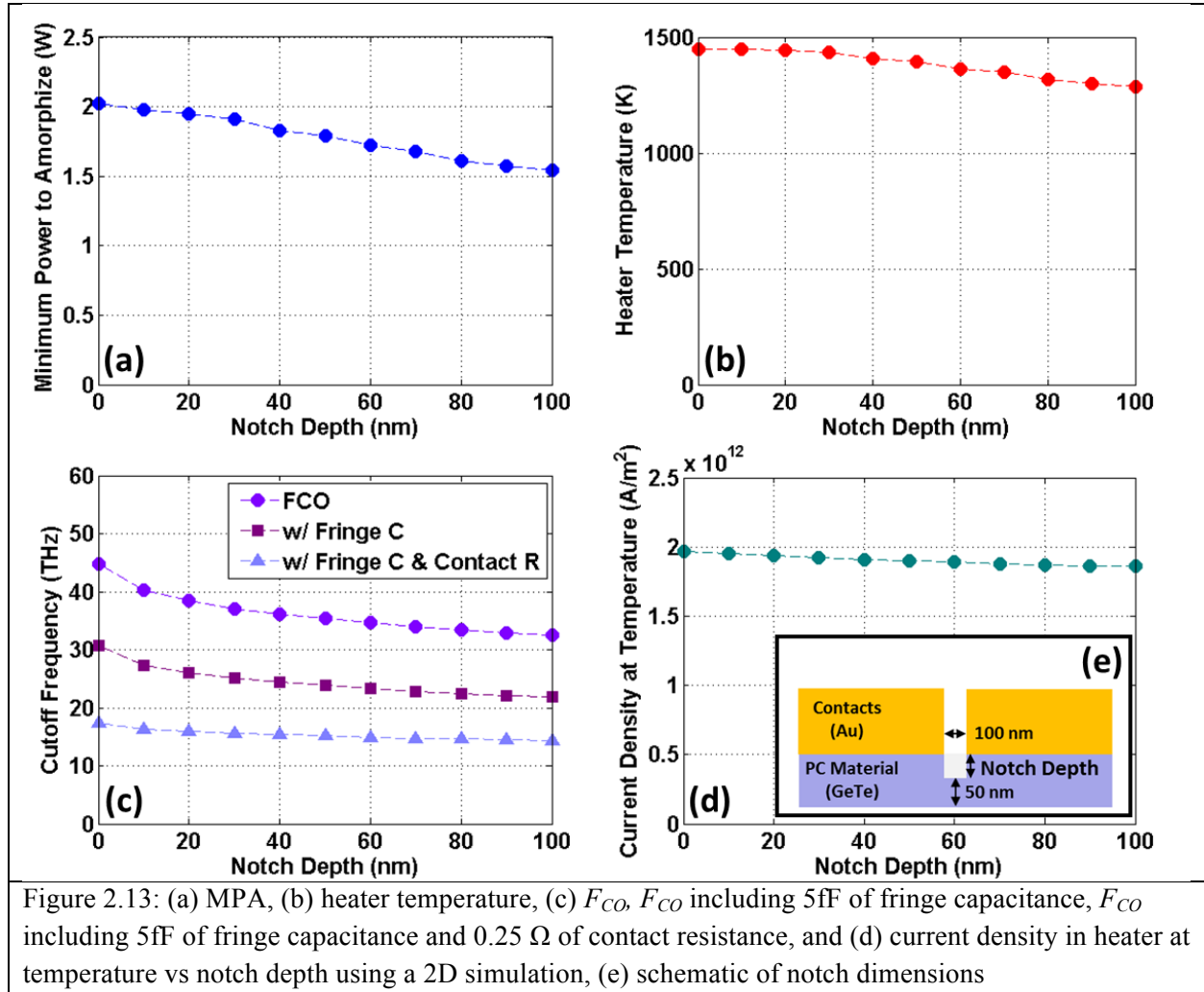
Without considering the effects of fringing capacitance and contact resistance, the highest performing simulated switch has F_{CO} of 45 THz and has a 1 μm wide heater with a 100 nm long RF gap. However, it has the highest MPA and requires over 2 W to melt the PC-material. The smallest RF gap also requires the heater to reach a temperature of almost 1500 K. In an effort to reduce the MPA, a notch can be made into the PC layer to limit the effect of the electrodes on shunting the heat flow. The notch is created by having a thicker PC layer and patterning the RF gap into the PC until it is 50 nm thick (fig. 2.12). The extra PC-material has a thermal conductivity of 1 W/m-K while still being electrically

conductive, which thereby allows the increased thermal gradients caused by the electrodes to be reduced in the PC-material under the notch. This reduces the MPA (fig 2.13(a)) and the temperature the heater (fig 2.13(b)) must achieve to melt the PC-material. As the notch depth increases, the MPA reduces from 2 W down to 1.5 W.



The F_{CO} also decreases with increasing notch depth (fig 2.13(c)). R_{ON} increases because the current flows through on-state PC material down to the notch, which results in the F_{CO} decreasing from 45 THz down to 32 THz. The decrease in F_{CO} is larger than the reduction in MPA, thus making the trade-off seemingly unnecessary. However, the addition of any fringing capacitance or contact resistance results in the F_{CO} being less affected by notch depth. This results in the notch having some benefit. The MPA decreases by 25% while the FCO with 5 fF of fringe capacitance and 0.25 Ω of contact resistance only reduces by 10%.

The current density in the heater decreases with increasing notch depth (fig 2.13(c)). However, this decrease is minimal and, even at a notch depth of 100 nm, is only reduced by less than 10%. The higher current density along with the higher heater temperature may reduce heater reliability and must be considered if heater durability is in question.



2.7.4 Barrier Layer Thickness

As previously discussed, the barrier layer between the heater and PC-material plays an important role in the performance of the switch. The barrier layer is needed to electrically isolate the RF signal path from the programming path while thermally connecting the heater to the PC material. AlN was chosen as the material for the barrier layer because it is thermally conductive while still being an electrical insulator. To further isolate the heater from the RF signal path, the barrier layer thickness can be increased. However, increasing the thickness of the barrier layer does have its consequences. A 2D model was simulated (fig. 2.14) to determine the effect of increasing the thickness of the AlN. The heater width and RF gap length remained constant at 1 μm and 500 nm, respectively.

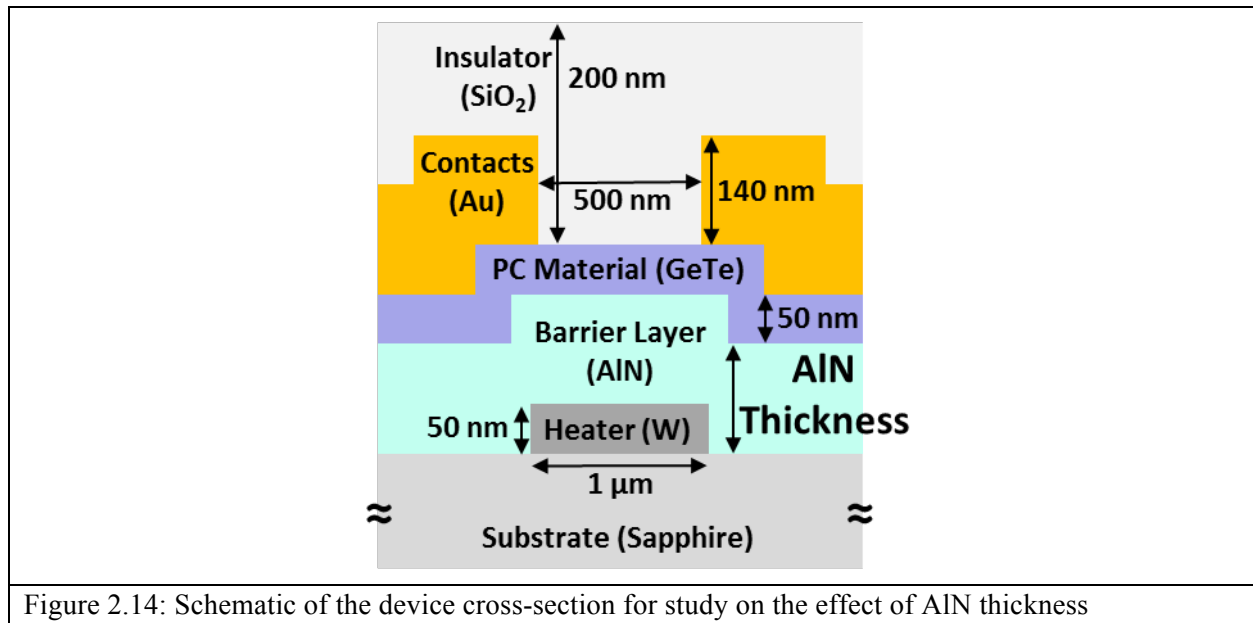


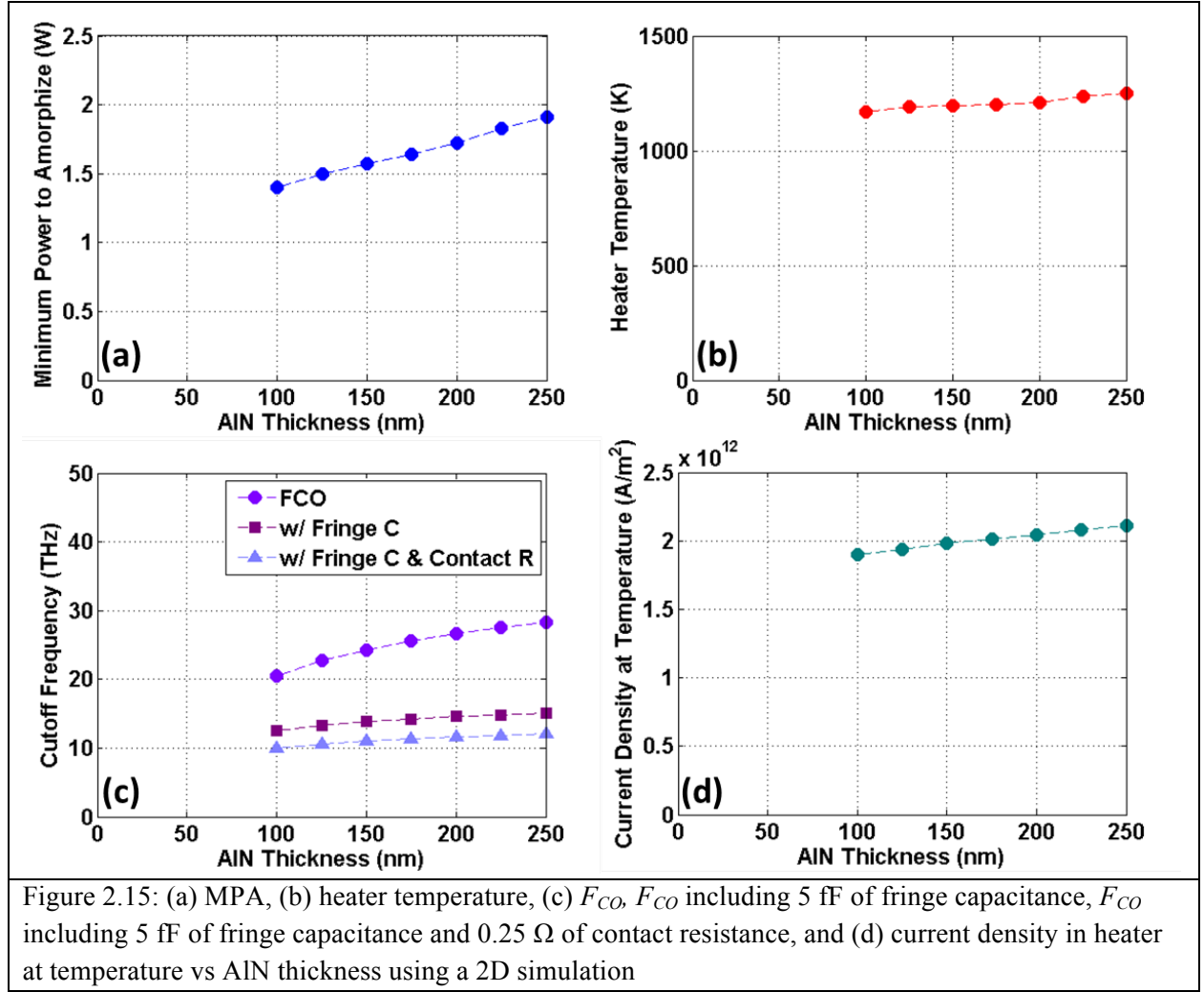
Figure 2.14: Schematic of the device cross-section for study on the effect of AlN thickness

As expected, the MPA increased with increasing AlN thickness (fig. 2.15(a)). However, not all of the increase in the power required to melt the top of the PC-material can be attributed to the additional thermal resistance between the heater and PC-material. The additional heat capacitance also contributes to the increase in MPA. The total volume that must be heated increases with thicker AlN layers, thereby increasing the thermal heat capacitance. Because MPA pulses are only 100 ns long, the increase in heat

capacitance reduces the speed at which the volume surrounding the heater increases in temperature. To overcome this, more power is needed to address the increase in heat capacitance. By using AlN as the barrier layer instead of SiN_x or SiO₂, the increase in MPA resulting from increased barrier layer thickness is reduced. The MPA only increases by 1/3 W per 100 nm of additional AlN.

The heater temperature increases slightly with increasing AlN thickness (fig. 2.15(b)), but the difference in temperature between the heater and the top of the PC-material only increases from 200 K to 250 K. This small increase further supports the claim that the rise in MPA is due mostly to the increase in heat capacity and not to the thermal resistance from the additional AlN thickness.

The F_{CO} increases with AlN thickness (fig. 2.15(c)) from 20 THz to 28 THz due to the reduction in C_{OFF} . An increase of almost 50% in F_{CO} resulted in only a 33% increase in MPA. However, the reduction in C_{OFF} due to increasing the AlN thickness begins to saturate after 250 nm, resulting in a maximum F_{CO} of 35 THz. Therefore, increasing the thickness of AlN past a certain point affects the MPA more than the F_{CO} . The maximum F_{CO} /MPA ratio occurs at 175 nm of AlN, making it the optimal thickness for the barrier layer. The addition of fringing capacitance and contact resistance diminishes the advantage of increasing the thickness of AlN. The gain in F_{CO} drops from 50% down to 20%, thus making it lower than the increase in MPA. Therefore, 100 nm of AlN is the ideal thickness for the barrier layer.



The current density in the heater increases slightly with increasing AlN thickness (fig. 2.15(b)). The increase in current density corresponds to the increase in MPA. However, the current density only increases by 10%. If the durability of the heater is in question, then this increase in current density may limit the thickness of the barrier layer that can be used in the switch.

2.7.5 The Effect of Pulse Length on MPA

The length of the amorphization pulse is not fixed. For the previous simulations, it was held constant at 100 ns in duration; however, increasing the length of the pulse can reduce the voltage required

to amorphize the switch [16] as well as the MPA. A 2D model of a standard switch (fig. 2.16) with a $1\text{ }\mu\text{m}$ wide heater, 100 nm of AlN and a 500 nm long RF gap is simulated using different amorphization pulse lengths ranging from 50 ns to $1\text{ }\mu\text{s}$.

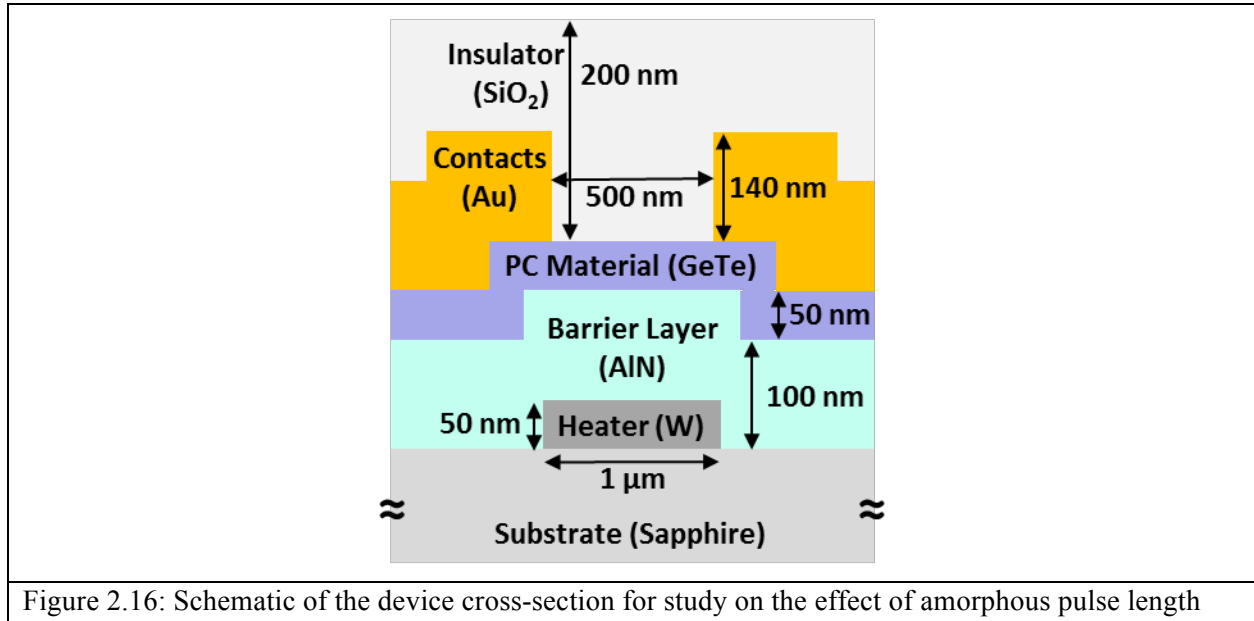


Figure 2.16: Schematic of the device cross-section for study on the effect of amorphous pulse length

As the pulse length increases, the MPA decreases (fig. 2.17(a)) significantly down to 0.8 W for a $1\text{ }\mu\text{s}$ long pulse. However, going beyond that pulse length does not result in a significant reduction in MPA. The heater temperature also decreases as a result of longer pulses (fig. 2.17(b)). The reduction in MPA and heater temperature is due to the heat capacity of the system becoming less of a determinant for longer pulses. However, increasing the pulse length does lead to an increased volume in the device being heated. Fig. 2.17(c) shows how deep the 473 K (crystallization temperature) contour line goes into the sapphire substrate. As the pulse width increases, the penetration depth into the substrate gets longer and does not plateau. This increase in penetration depth and heated volume leads to an increase in cooling time of the PC-material at the top of the switch (fig. 2.17(d)) which could lead to the inability to quench the molten PC-material quickly enough for it to become amorphous. If the crystallization time is shorter than cooling time, the switch will never be able to turn off. Therefore, the MPA can only be reduced up to a certain point.

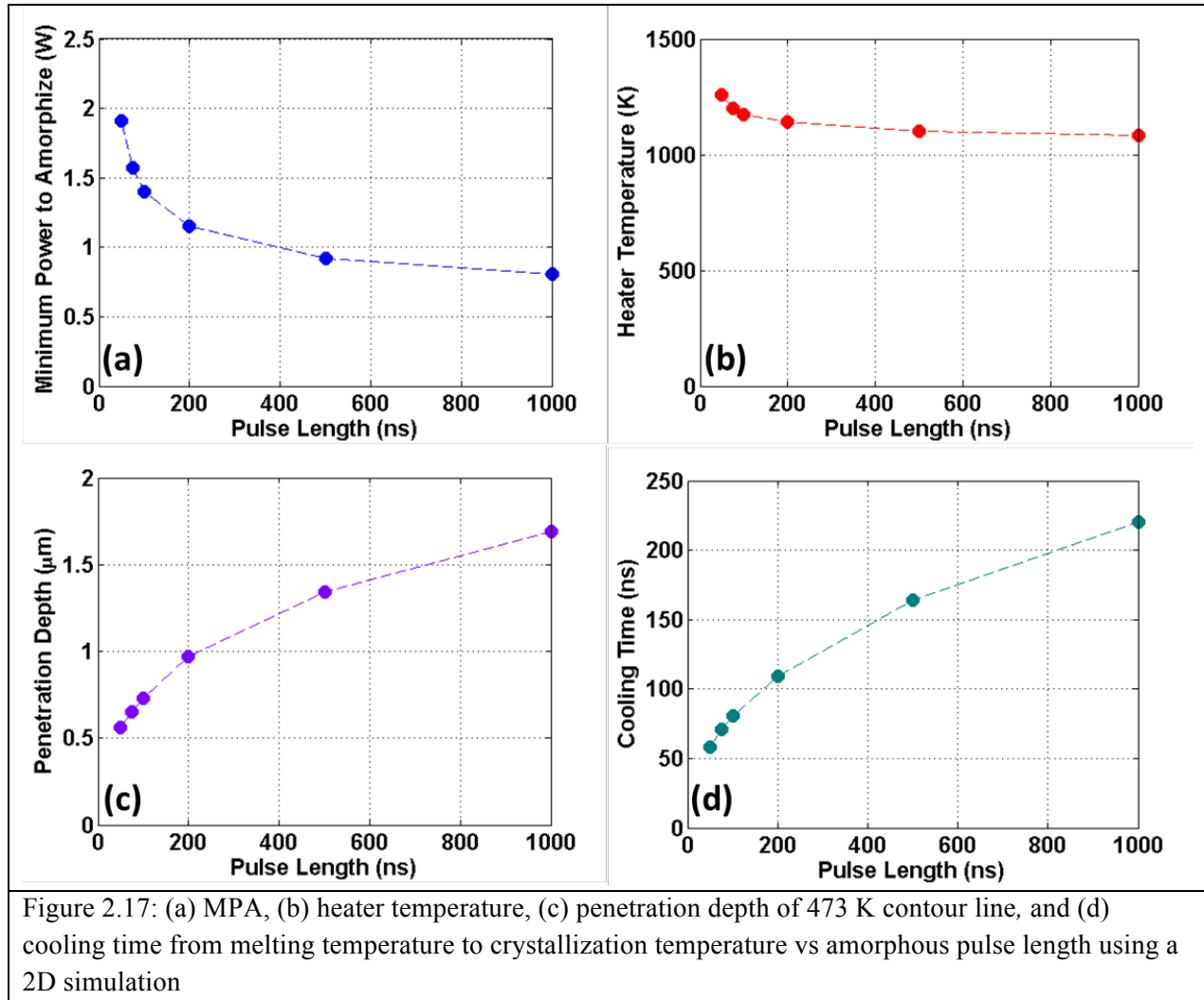
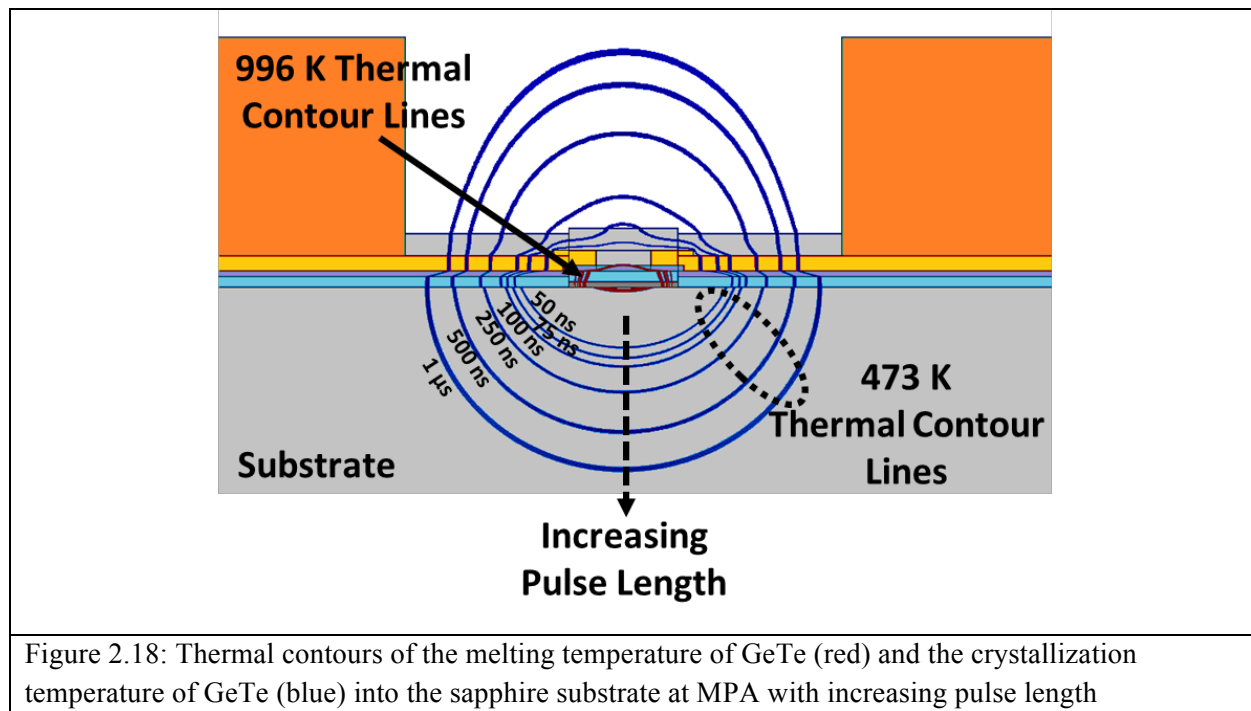


Fig. 2.18: shows the thermal contours for 996 K (red) and 473 K (blue) at the end of the MPA pulse for each pulse length. The area inside the red contour lines is hot enough to melt the PC-material and needs to be cooled below the crystallization temperature (473 K). The area inside the blue contour lines is above the crystallization temperature and represents the increased volume into the substrate that must be cooled. This suggests that if the crystallization time of the PC-material is faster than the cooling time, a shorter pulse with more power may be used to turn the switch off if longer pulses cannot do so. Crystallization times of less than 150 ns are assumed to be fast enough for this work.



2.8 Summary

There are many factors to consider when designing, modeling and simulating a 4-terminal inline RF phase change switch. The choice of PC-material and material for the barrier layer is critical for maximizing the performance of the switch. In this work, GeTe was chosen as the PC-material because of its low resistivity in the ON-state ($1.68 \mu\Omega\text{-m}$) and AlN was chosen for the barrier layer due to its high thermal conductivity (285 W/m-K) as compared to other dielectrics such as SiN_x .

Including the temperature dependence of sapphire's thermal conductivity and heat capacity as well as a thermal interface between the W heater and sapphire substrate was necessary to ensure the model's accuracy. The use of 2D models could be substituted for larger 3D models to save on computing power without sacrificing simulation accuracy. The heat of fusion of GeTe was not included in the simulation results due to its difficulty to implement in the model. The heat of fusion increases the required energy to melt the GeTe and as a result the simulated MPAs reported underestimates the actual power required to amorphize the GeTe. However, the volume of GeTe that is melted only accounts for

10% of the total heated volume, and thus the heat of fusion will only increase the simulated MPA by 10%.

When designing a 4-terminal inline RF phase change switch, there are three main design points that must be considered. RF gap length, the use of a notch and the thickness of the AlN barrier layer all trade off power for increased performance. Minimizing the heater width not only improves performance but also reduces power consumption. Therefore, using the narrowest heater is ideal unless it reduces heater reliability. If there is not any limitation on power, a switch with a short RF gap and thick AlN layer would yield the best performance. Even when considering power, an RF gap of 100 nm has the highest F_{CO} /MPA ratio for all the devices simulated. When 5 fF of fringe capacitance is added, a 100 nm RF gap still has the highest F_{CO} /MPA ratio. However, when 0.25 Ω of contact resistance is also included, the use of a 100 nm deep notch with a 100 nm RF gap results in the highest F_{CO} /MPA ratio. All of these conclusions are based upon a 20 μ m wide switch and would vary slightly for switches of different widths. While contact resistance would scale with the switch width, the fringe capacitance would not.

The advantage of a notch is apparent for situations in which there is fringing capacitance and contact resistance. However, in the other cases it may seem to add unnecessary complexity. If the design was limited by having only 1.6 W of available power, a switch with either 300 nm long RF gap with no notch or one with a 100 nm long RF gap and 100 nm notch could be used. The switch with a 300 nm RF gap would have an F_{CO} of 27.5 THz, while the switch with the notch would have an F_{CO} of 32.5 THz. Even with the addition of fringing capacitance and contact resistance, the switch with the notch would always have a higher F_{CO} . Therefore, the use of a notch can reduce power without sacrificing as much performance as would be incurred by increasing the RF gap length.

Chapter 3: Phase Change RF Switch Fabrication

3.1 Abstract

Manipulating the device design is important in maximizing switch performance, but it can only go so far. Improving the materials used in the switch allows for additional improvements in performance that cannot be achieved by just reducing the RF gap length or heater width. In this chapter, three major contributions to the materials used in the switch are detailed. The introduction of a low resistivity W heater (75 n Ω -m), high-thermal conductivity barrier layer (\sim 50 W/m-K) and lowest demonstrated GeTe resistivity (1.5 $\mu\Omega$ -m) result in the F_{CO}/MPA ratio doubling from 7.8 THz/W to 15.6 THz/W when compared to the materials used in the current state-of-the-art PC switch [15].

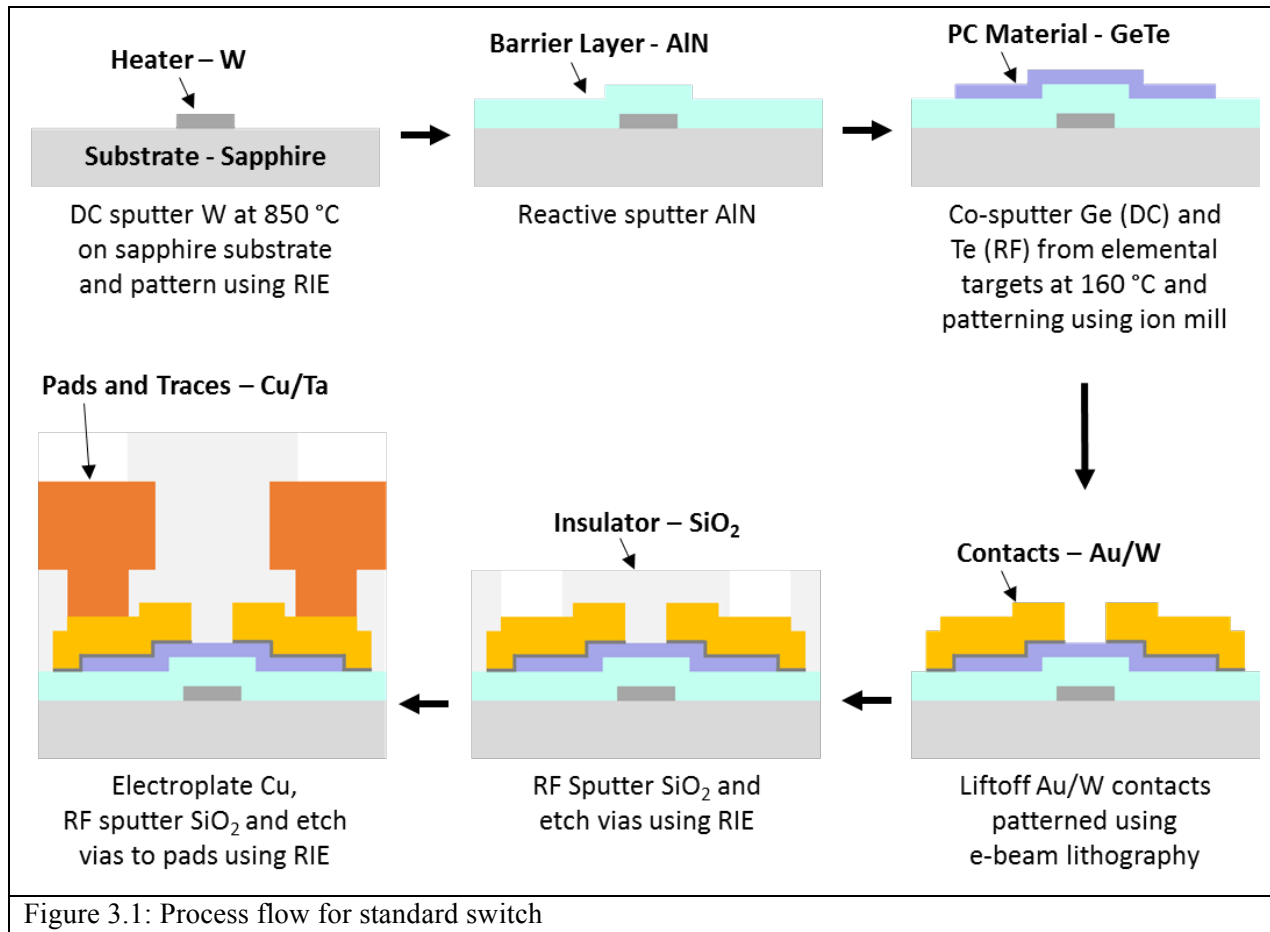
3.2 Introduction

Improving the electrical and thermal properties of the switch are important to further increase its performance. The current state-of-the-art RF PC switch [15] uses a high resistivity NiCrSi heater (1500 n Ω -m), low thermal conductivity SiN_x barrier layer (\sim 1 W/m-K) and has a GeTe resistivity of 3.6 $\mu\Omega$ -m. Reducing the GeTe resistivity has the most direct impact on RF performance. The use of a higher thermal conductivity barrier layer such as AlN would allow for a reduction in MPA while reducing OFF-state capacitance. Changing the heater material used from NiCrSi to W allows for reduction in actuation voltage due to a reduction in resistivity.

This chapter will discuss the fabrication process of a standard 4-terminal inline RF phase change switch as well as one with a notch. In addition, three major advancements in materials used over prior works will also be discussed: W heaters, an AlN barrier layer and low resistivity GeTe.

3.3 Standard Switch Process Flow

Fig. 3.1 shows the process flow for a standard switch. As discussed in the previous chapter, the switch is built on a sapphire substrate. To prepare it for the first layer, the sapphire substrate is placed in a beaker of acetone and sonicated for 10 minutes. It is then rinsed with acetone and isopropyl alcohol (IPA). The substrate is cleaned in the O₂ plasma asher for 1 minute to remove any organic residue that might remain.



The sapphire substrate is then heated and maintained at 850° C while W is deposited using DC magnetron sputtering for 1800 seconds yielding approximately 70 nm of W. Once the deposition is complete, the substrate is allowed to cool to about 40 °C inside the vacuum chamber. The sample is then patterned using 1 μm of photoresist. It is necessary to use a 10 minute Hexamethyldisilazane (HMDS)

vapor prime on the sample prior to spin coating it with photoresist. The HMDS vapor prime is required for the photoresist to adhere to the W film and prevent alignment marks from washing away during development. The W is etched using a CHF_3 and O_2 gas chemistry in a parallel plate reactive ion etcher (RIE). The photoresist is removed by a thorough cleaning in the O_2 plasma asher for 3 minutes followed by a 10 minute sonication in acetone. This process ensures that no photoresist residue remains on the heaters.

After the heaters are patterned, the next step is to deposit the 100-200 nm thick AlN barrier layer. The surface of the sample is first cleaned using a 1 minute sputtered etch. Then AlN is reactively sputtered from Al targets in a nitrogen rich environment using an S-Gun configuration [57]. Two doughnut shaped Al targets sputtered using AC magnetron sputtering (40 kHz) are used to prevent the disappearing anode effect that is present in DC reactive sputtering. The sputtering environment is N_2 rich which causes “poisoning” of the Al target where the AlN is being formed on its surface and then sputtered off onto the substrate. As a result of this sputtering process, polycrystalline AlN is deposited on the sample.

After the deposition of the AlN barrier layer, a 50-100 nm thick phase change layer is deposited. The PC-material is co-sputtered from elemental Ge and Te targets. The Ge uses DC magnetron sputtering while the Te uses RF magnetron sputtering. RF magnetron sputtering is used for Te to reduce the sputtering rate to one similar to that of Ge. The sputtering conditions used are critical in minimizing the resistivity of the GeTe and will be discussed later in the chapter. Before the deposition takes place, the substrate is heated to 160°C . A 1 minute sputter etch is performed to clean the surface of the sample. After the sputter etch is completed, the GeTe is then deposited. The sample remains in the vacuum chamber to cool down before it is removed. The deposition temperature of 160°C was experimentally determined and will be discussed in further detail later in the chapter. A $1\text{ }\mu\text{m}$ thick photoresist layer is used to pattern the GeTe. The photoresist also has difficulty adhering to the GeTe and, therefore, a 10 minute HMDS vapor prime is required before the sample is coated the photoresist. The GeTe is

etched using an Ar^+ ion mill. After ion milling, the surface of the photoresist becomes hard and is difficult to remove. Therefore, it is necessary to first thoroughly clean it in the O_2 plasma asher for 3 minutes followed by a 10 minute sonication in acetone to remove the photoresist.

Once the GeTe is patterned, the Au contacts are created using a lift-off process. This layer uses electron beam lithography to pattern the area where Au contacts are to be deposited. A $1\text{ }\mu\text{m}$ thick PMMA A7 ebeam-resist is spin coated onto the sample. Because the sapphire substrate is electrically insulating, a thin 10 nm layer of Al is deposited on top of the resist to minimize charging. The patterns are written using a 30 kV beam voltage with a beam current between 25-30 pA. The resist is exposed with a dose of $300\text{ }\mu\text{C}/\text{cm}^2$. After the exposure of all of the devices is completed, the Al layer on top of the resist is removed by dipping the sample in diluted AZ400K developer solution for 30 seconds. Once the Al layer is removed, the resist can be developed using a 1:3 MIBK/IPA solution for 1 minute followed by a dip in IPA for 15 seconds. Next, a low power 2 minute descum in the O_2 plasma asher is conducted to remove any residual ebeam resist that maybe present in the contact windows. The sample is then placed in the vacuum chamber where the sample surface is sputter etched for 3 minutes before the metallization is deposited. After the sputter etch, 10 nm of W is deposited using DC magnetron sputtering followed immediately by 130 nm of Au, also using DC magnetron sputtering. Once the deposition is completed, the sample is the sonicated in acetone for 10 minutes or until all of the W/Au metal is lifted off.

The next step is to deposit a 100 nm thick protective SiO_2 layer over the entire sample. This layer is needed to protect the GeTe in the RF gap from being etched when the Cu seed layer is removed after electroplating the pads and traces. The SiO_2 layer is deposited using RF magnetron sputtering. A $1\text{ }\mu\text{m}$ thick photoresist is spun onto the sample and the vias are exposed over the Au contacts. Vias in the SiO_2 are etched using a CHF_3 and O_2 gas chemistry in a parallel plate RIE. The photoresist is then removed.

In order to make electrical contact to the heater pads, vias are etched into the AlN barrier layer. A $1\text{ }\mu\text{m}$ thick photoresist is spun onto the sample and the vias are exposed over the W heater pads. The

AlN is etched using an inductively coupled plasma (ICP) RIE. The gas chemistry used for the etch is 25% Cl_2 , 5% BCl_3 and 70% Ar. After the etch is completed, the photoresist is removed using a thorough clean in the O_2 plasma asher for 3 minutes followed by a 10 minute sonication in acetone.

After the vias are etched in the SiO_2 and AlN, the seed layer for electroplating the pads and traces is deposited. First, the sample is sputter etched for 5 minutes to ensure good electrical contact to the Au. Then, 10 nm of Ta followed by 100 nm of Cu are deposited using DC magnetron sputtering. Next, 2 μm of photoresist is spun onto the sample and the pads and traces are exposed. A low power 2 minute descum in the O_2 plasma asher is used to remove any residual photoresist that maybe present on the exposed Cu seed layer. The sample is then placed in a Cu electroplating bath. Using a pulsed power supply, with 15 ms of forward current and 1 ms of reverse current per pulse, for 20 minutes results in 2 μm of plated Cu. Once the plating is completed, the photoresist is stripped and the Cu/Ta seed layer is removed using an Ar^+ ion mill.

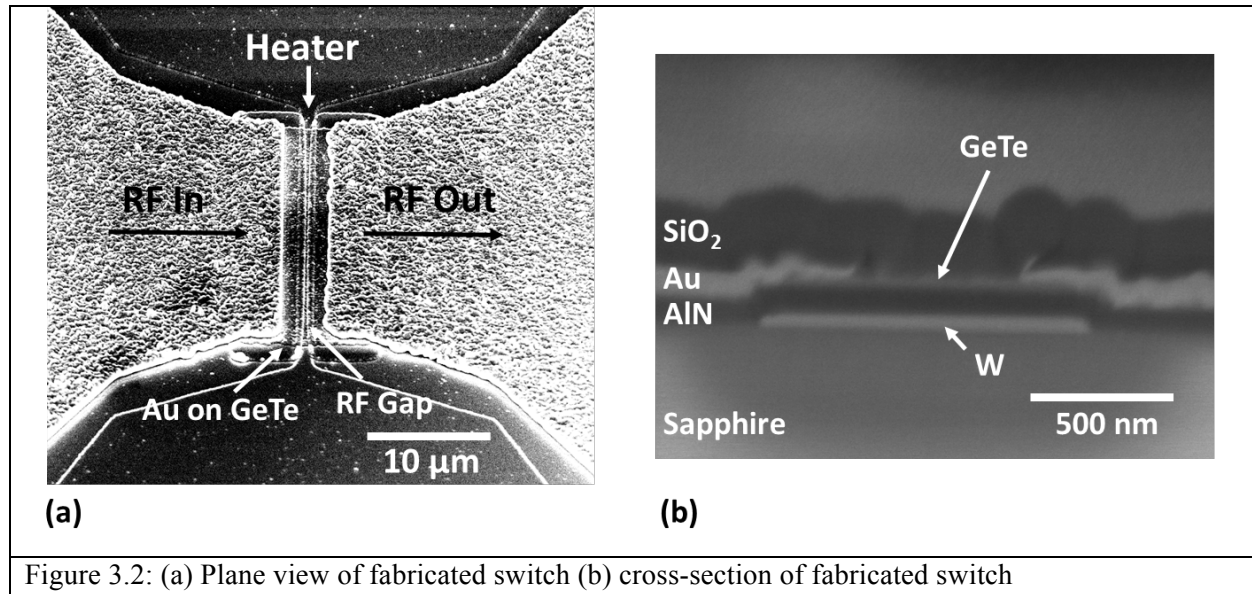


Figure 3.2: (a) Plane view of fabricated switch (b) cross-section of fabricated switch

The next step is to deposit a 100 nm thick SiO_2 protective layer over the sample using RF magnetron sputtering. A 1 μm thick photoresist is spun onto the sample and the vias are exposed over the plated Cu pads. Vias in the SiO_2 are etched using a CHF_3 and O_2 gas chemistry in a parallel plate (RIE) and the photoresist is then removed. A finished device and its cross-section are shown in fig. 3.2. A W heater runs vertically in fig. 3.2(a) directly on the sapphire substrate (fig. 3.2(b)). A 100 nm thick AlN barrier layer separates the W heater and GeTe (fig. 3.2(b)). The RF gap (fig. 3.2(a)) is defined by the space between the Au contacts onto of the GeTe as seen in fig. 3.2(b).

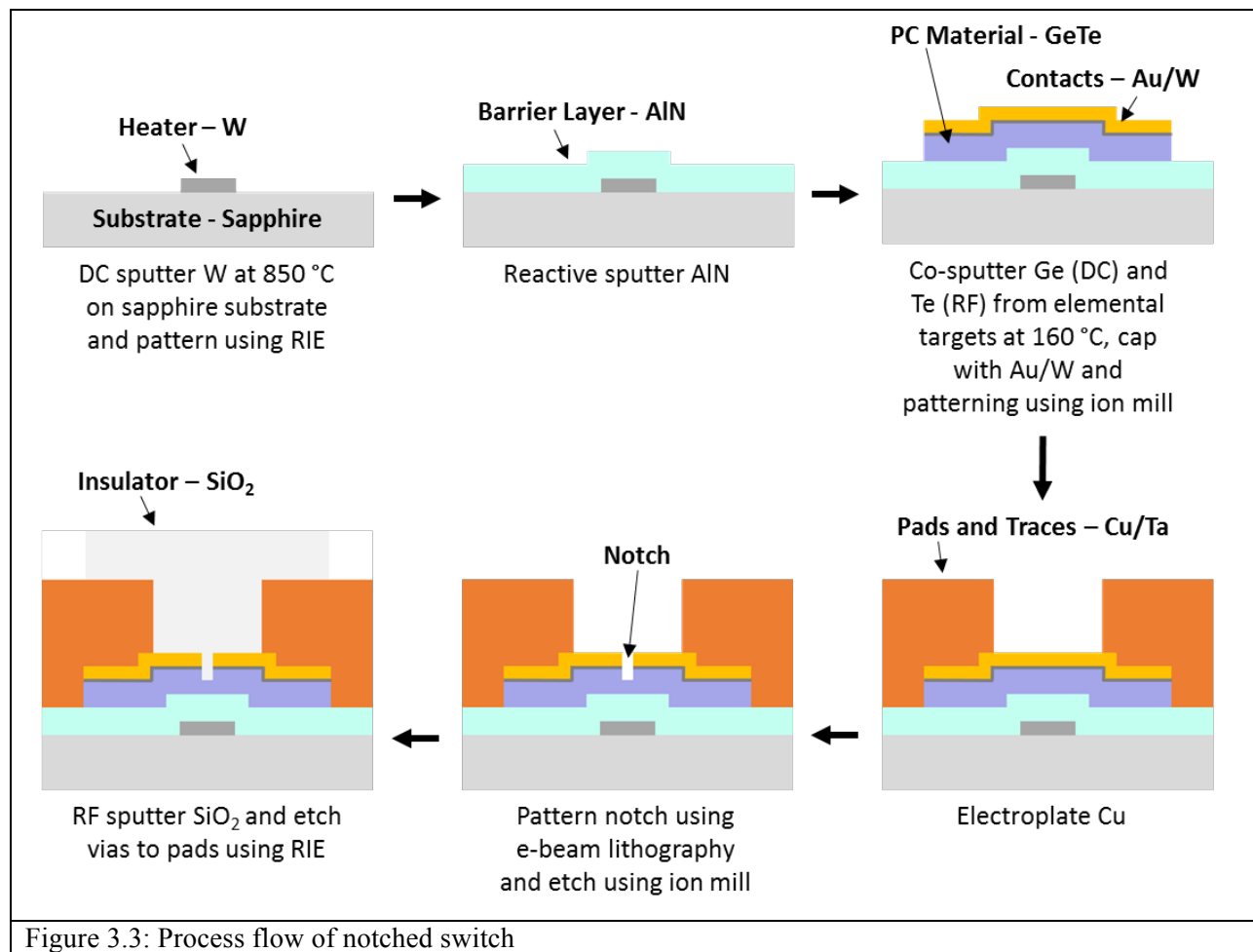


Figure 3.3: Process flow of notched switch

3.4 Notched Switch Process Flow

The initial steps of the process flow for fabricating a 4-terminal inline RF phase change switch with a notch are the same as those for the standard switch for the heater and barrier layers (fig. 3.3). The patterning of the RF gap and notch are the last steps in the process. The sapphire substrate is cleaned and prepared in the same way as the standard switch. A 70 nm W film is deposited at 850 °C and the heaters are patterned using a CHF_3 and O_2 gas chemistry in the RIE. Next, the sample is sputter etched for 1 minute before 100-200 nm of AlN is deposited on the sample.

After the AlN barrier layer is deposited, a film stack of GeTe, W and Au is deposited without the sample breaking vacuum. This is done by first heating the substrate to 160 °C and cleaning the sample surface with a 1 minute sputter etch. After the sputter etch, 150 nm of GeTe is sputtered using the same co-sputtering technique as discussed earlier followed by 10 nm of W and 130 nm of Au. By depositing the entire stack without the sample breaking vacuum, a pristine interface is present between the GeTe layer and contact metal. This helps minimize any contact resistance (R_{PC}) at this interface due to contamination. The whole stack is patterned by spin coating 1 μm of photoresist and etching it in an Ar^+ ion mill. The photoresist is removed using a thorough clean in the O_2 plasma asher for 3 minutes followed by a 10 minute sonication in acetone to ensure no photoresist residue remains.

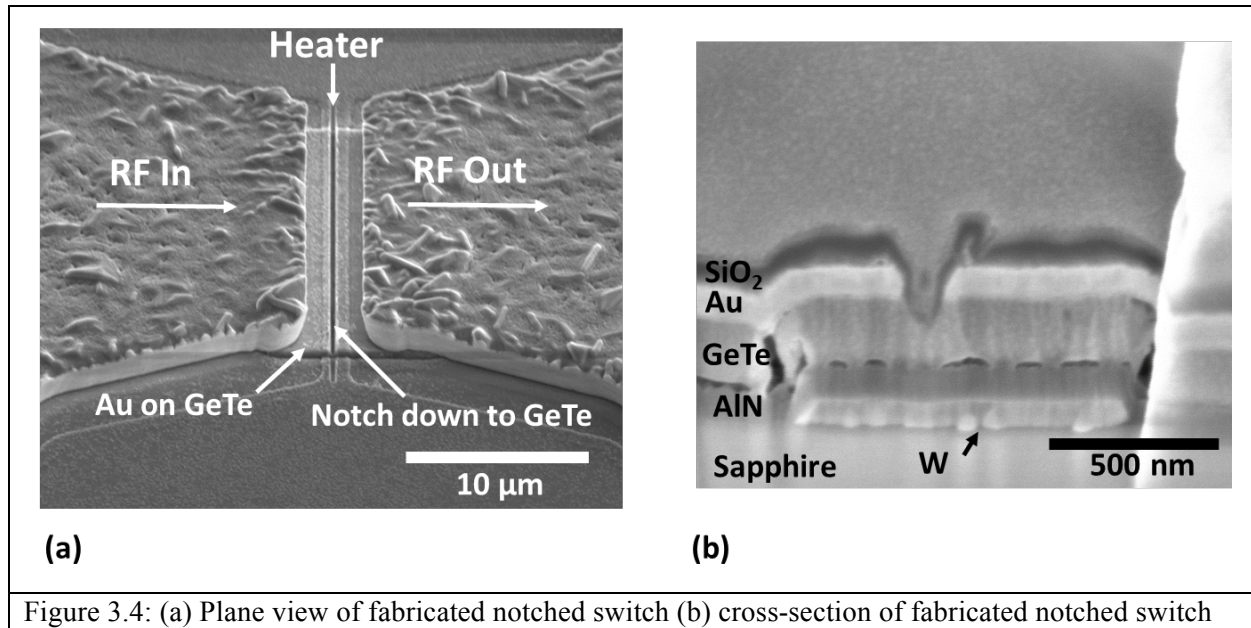
Once the film stack is patterned and etched, the vias in the AlN barrier layer also must be etched in order to make electrical contact to the heater pads. A 1 μm thick photoresist is spun onto the sample and the vias are exposed over the W heater pads. The AlN is etched using same ICP RIE recipe used in the standard switch. The photoresist is removed using a thorough clean in the O_2 plasma asher for 3 minutes followed by a 10 minute sonication in acetone.

After the vias in the AlN are made, the surface of the sample is sputter etched for 5 minutes before the Ta/Cu seed layer is deposited. The traces and pads are patterned using 2 μm of photoresist

followed by 2 μm of plated Cu. The photoresist is stripped and the Ta/Cu seed layer is removed using an Ar^+ ion mill.

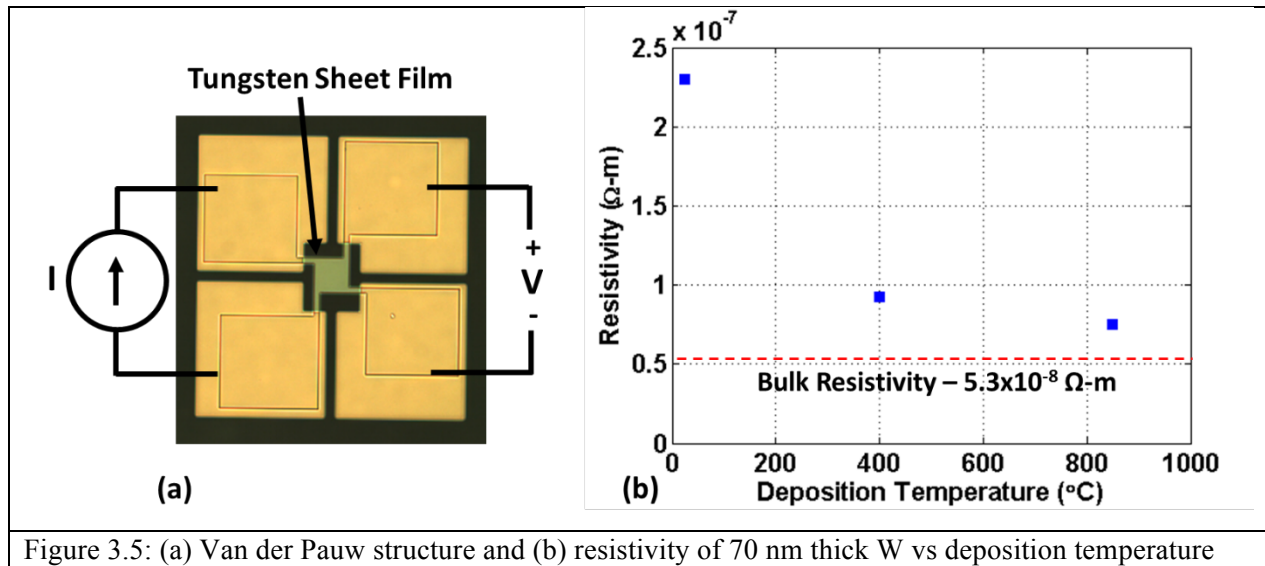
The next step is to define the RF gap and etch the notch in the GeTe. The RF gap is patterned using e-beam lithography. A 200 nm thick ebeam resist layer is spun onto the sample using PMMA A2. A 10 nm thick layer of Al is deposited on top of the ebeam resist to prevent charging in the SEM. A 100 nm wide line is patterned along the length of the heater using a $700 \mu\text{C}/\text{cm}^2$ dose and the same e-beam conditions described earlier. After all of the devices are exposed, the Al is dissolved using diluted AZ400K and then developed in MIBK/IPA 1:3 for 60 seconds followed by a 15 second dip in IPA. Once the RF gap is patterned, an Ar^+ ion mill is used to etch through the Au, W and into the GeTe until only 50 nm remain. The ebeam resist is then removed by sonicating the sample in acetone for 10 minutes.

The final step is to deposit 200 nm of SiO_2 as a protective layer and then etch vias down to the pads. The SiO_2 is deposited using RF magnetron sputtering. A $1 \mu\text{m}$ thick photoresist layer is spun onto the sample and vias are exposed and developed over the Cu pads. Vias in the SiO_2 are etched using a CHF_3 and O_2 gas chemistry in a parallel plate RIE. The photoresist is then removed. A finished notched device and its cross-section are shown in fig. 3.4.

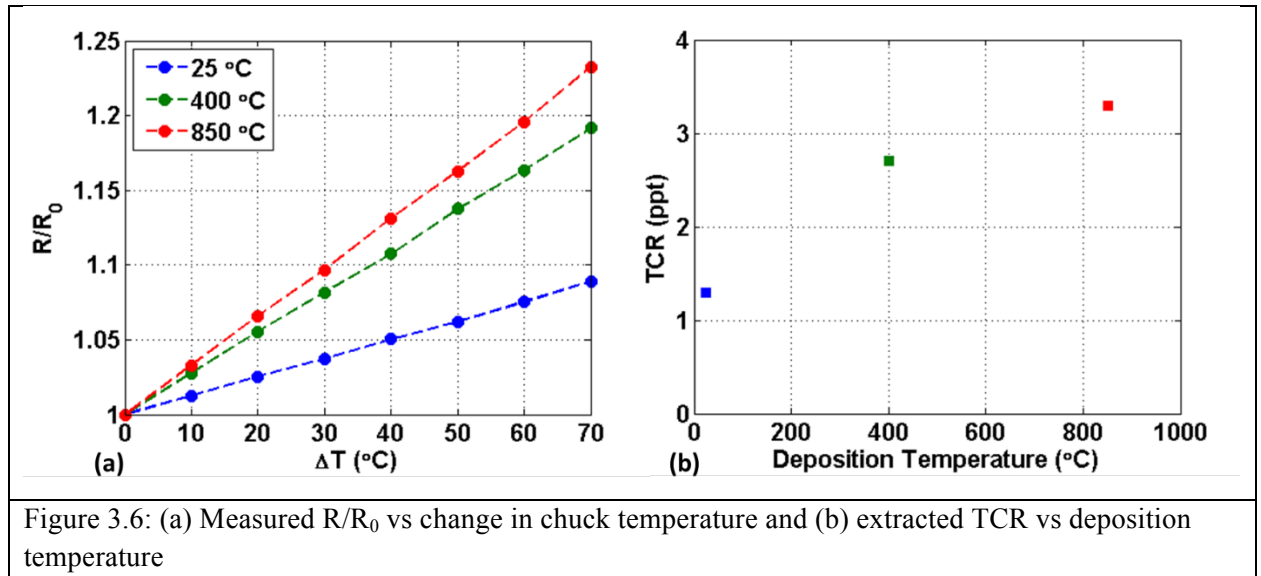


3.5 Low Resistivity Tungsten Heater

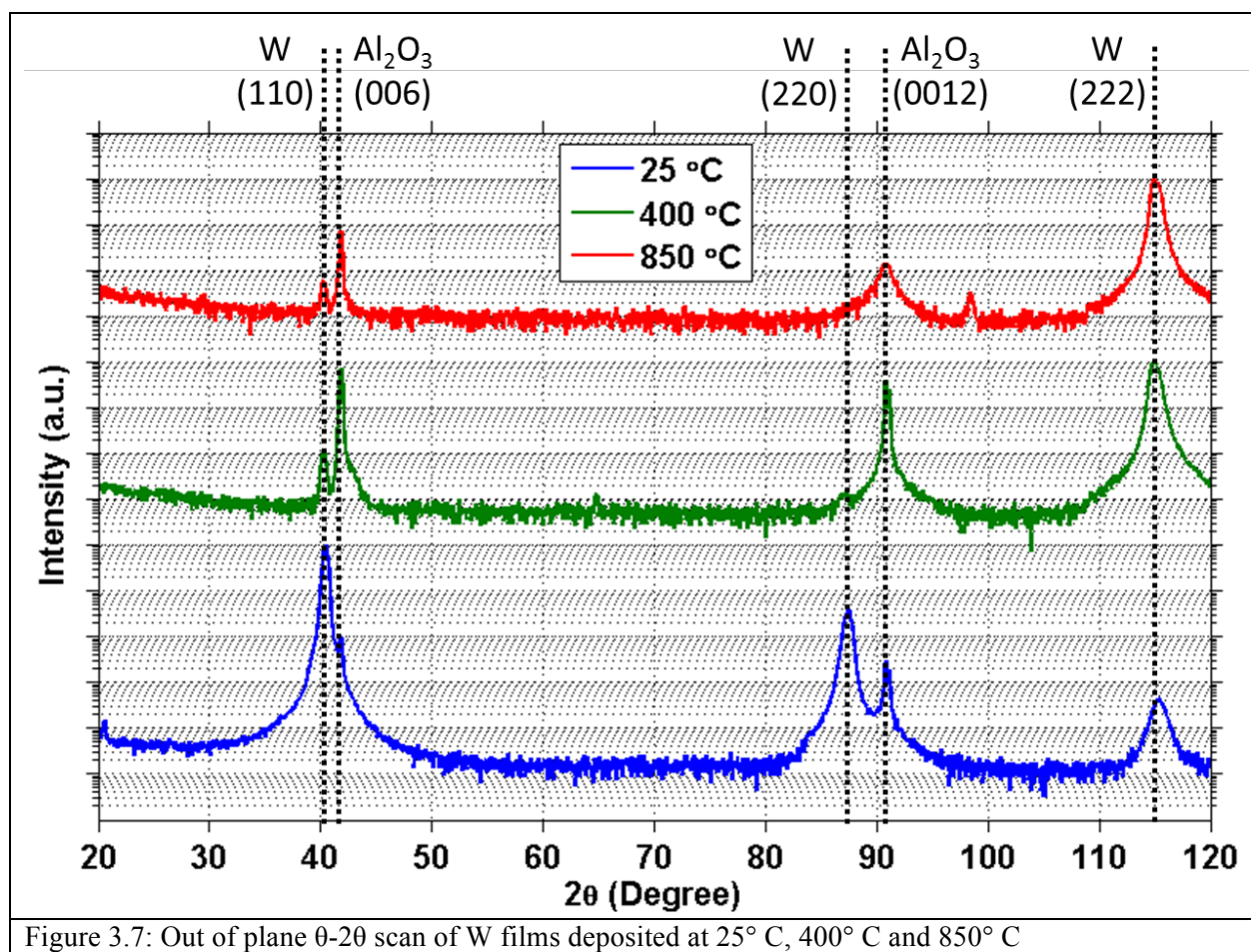
Depositing the W at an elevated temperature is critical to reducing the resistivity of W [58], [59]. To assess the required temperature and the role of temperature in determining resistivity, three W films were sputtered on c-axis sapphire substrates with one at each of the following temperatures: room temperature (25° C), 400° C and 850° C. The 400° C temperature was chosen because it is slightly less than the maximum post-processing temperature for CMOS wafers (450 -575° C) [60], [61]. The 850° C temperature was chosen because it is the maximum temperature the substrate can be heated to in the deposition system. All three films were sputtered using the same conditions: 50 W of DC power with 60 sccm of Ar at 3 mTorr for 1800 seconds resulting in a 70 nm thick film. Van der Pauw structures were patterned into the W using a fluorine based RIE followed by the liftoff of Cu pads for probing (fig. 3.5(a)). The Van der Pauw structures were used to measure the resistivity of the three films (fig. 3.5(b)). As the deposition temperature increases, the resistivity of the W drops from 230 nΩ-m at room temperature down to 75 nΩ-m at 850 °C. The resistivity of the W deposited at 850 °C is less than 50% greater than bulk (53 nΩ-m [58]) while the room temperature tungsten is over 4 times that of bulk. The W that is deposited at 450° C is almost as good as the W deposited at 850° C, but it allows for greater process flexibility due to its lower deposition temperature.



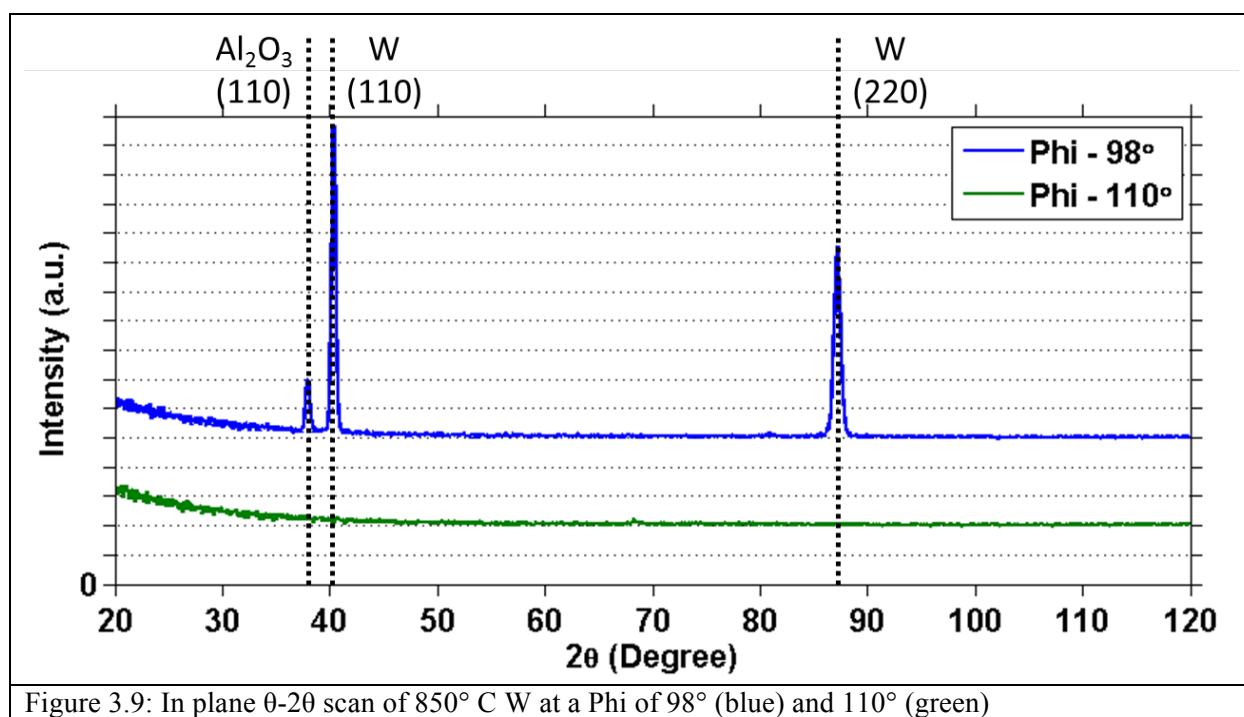
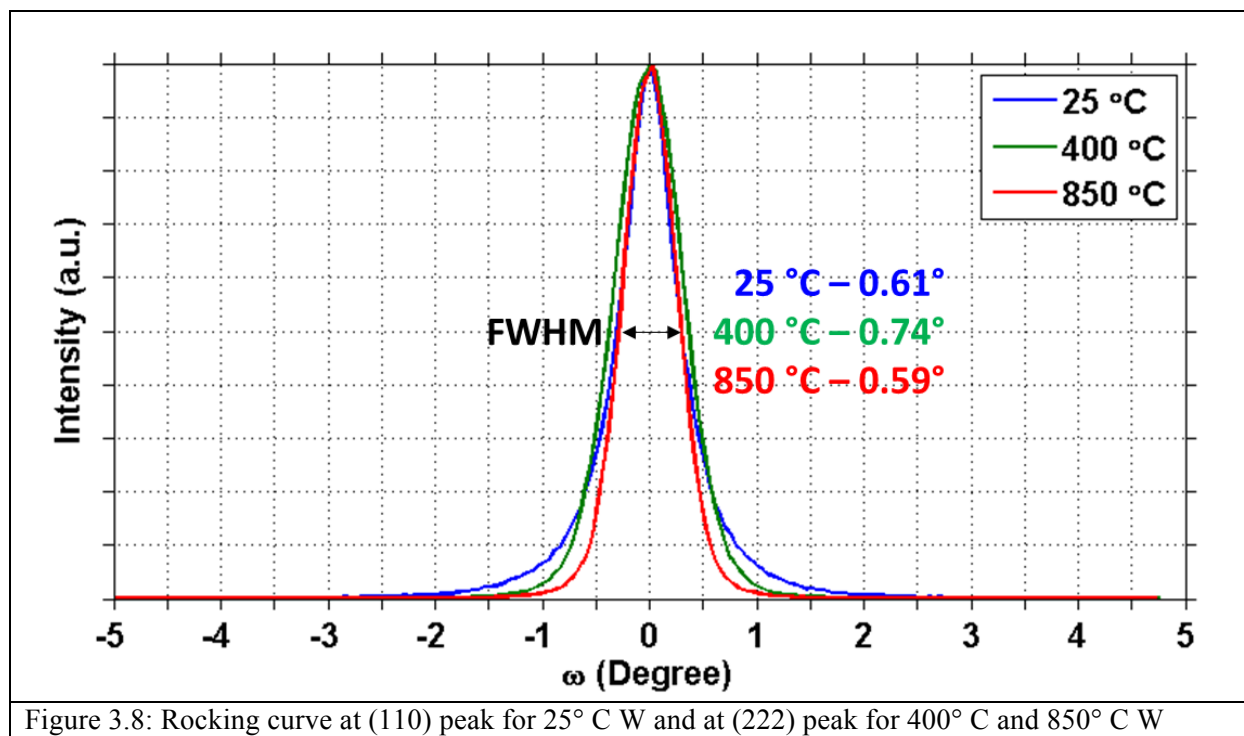
The TCR of the tungsten was extracted by measuring the resistance of the Van der Pauw structure from 25 °C to 95 °C, in 10 °C increments, using a heated temperature stage. The ratio of resistance at temperature divided by the reference resistance at 25 °C was plotted compared to changes in stage temperature (fig. 3.6(a)). The slope of the resulting line is the TCR of the W film. The slope of the line increases with temperature and almost triples in value when the W is deposited at elevated temperature (fig. 3.6(b)).



The crystal orientation of the 3 tungsten films were measured before they were patterned using XRD. An out of plane θ - 2θ scan was measured from 20° to 120° for the 3 films (fig. 3.7). The room temperature W film showed a large peak at the (110) and (220) angles. Once the deposition temperature is increased, there is no longer a peak at the (110) and (220) angles but it occurs instead at the (222) angle. This shows that by sputtering at elevated temperatures, the orientation of the sputtered W changes from being (110) to (111).



The rocking curve was then measured at the (110) peak for the W deposited at room temperature and at the (222) peak for the W deposited at elevated temperatures (fig. 3.8). The FWHM of all three films are less than 1° , which shows that they are all highly oriented films. While the W film deposited at room temperature is mostly likely fiber texture, an in plane scan was measured on the W film deposited at 850 °C to determine whether it was single crystal. The sample was rotated to a Psi angle of 89° and a quick Phi scan was measured on the (110) peak for sapphire. A (110) peak was found at a Phi of 98° . The sample was aligned to this peak and a θ - 2θ scan was measured at a Phi of 98° and 110° (fig 3.9). When Phi was 98° , three peaks are seen: sapphire (110), W (110) and W (220). When Phi is rotated to 110° , there are no peaks that can be seen. This measurement result means that the (111) W is epitaxially grown on the c-axis sapphire and that the W film may be pseudo-single crystal.



The reduction in resistivity due to depositing the film at elevated temperatures is not due to the crystal orientation of the W film. In D. Choi et. al., a similar resistivity was achieved by growing the W on a-plane sapphire to achieve a (110) texture [58]. The reduction in resistivity is most likely due to a decrease in grain boundaries and impurities in the film. The base pressure in the sputtering chamber has also been seen to affect the resistivity of the film even when sputtered at elevated temperatures. All of the films in this study we deposited at a base pressure $< 1 \times 10^{-8}$ Torr before the heater is turned on.

Table 3.1 shows the simulation results of a standard switch for 3 different W films as well as NiCr. As expected, the heater resistance decreases with W deposition temperature and, as a result, so does the V_{App} required to amorphize the switch. The MPA is also larger for the room temperature W film despite the higher heater resistance. Even though the TCR is higher for the films deposited at elevated temperature, the resistance of the heater when it is at the temperature required to melt the PC-material is still lower. All three tungsten films are an improvement over the NiCrSi used by N. El-Hinnaway et al., [16] which requires a 17 V pulse to turn off the switch. The low resistivity tungsten is necessary if the heaters are to be powered by an on-chip CMOS driver that has a maximum voltage supply of 3.3 V. Reducing the switch width and placing heaters in parallel as well as increasing the heater thickness will allow for further reduction in the required actuation voltage. The use of a W heater deposited at elevated temperatures may not appear to significantly reduce V_{App} . However, it does significantly reduce the resistance of the heater at temperature by 40%. This reduction is necessary if the actuation voltage is fixed at 3.3 V.

Deposition Temperature (°C)	Resistivity (nΩ-m)	TCR (ppt)	Heater Resistance (Ω)	V_{App} (V)	MPA (W)	Heater Temperature (K)	Heater Resistance @ Temperature (Ω)	J @ Temperature (A/m ²)
25	230	1.3	121	9.6	1.53	1273	245	1.30×10^{12}
400	92.4	2.7	52.2	8.5	1.44	1239	153	1.67×10^{12}
850	75.2	3.3	43.6	8.4	1.40	1238	144	1.73×10^{12}
NiCr	1500 [62]	0.4 [62]	850	18.6	1.45	1189	1084	6.56×10^{11}

Table 3.1: Simulation results of standard switch for the 3 different W films and NiCr as heater

3.6 AlN Barrier Layer

In the previous chapter, the importance of selecting an appropriate barrier layer for the switch was discussed. In previous work, a SiN_x barrier layer was used between the heater and the PC-material [15], [16], [38]. The measured thermal conductivity of this SiN_x layer was 1.1 W/m-K. A standard switch was simulated using SiN_x as the barrier layer with different thickness and compared to AlN (fig. 3.10). This simulation proves that the integration of AlN as the barrier layer in the switch is a significant advancement.

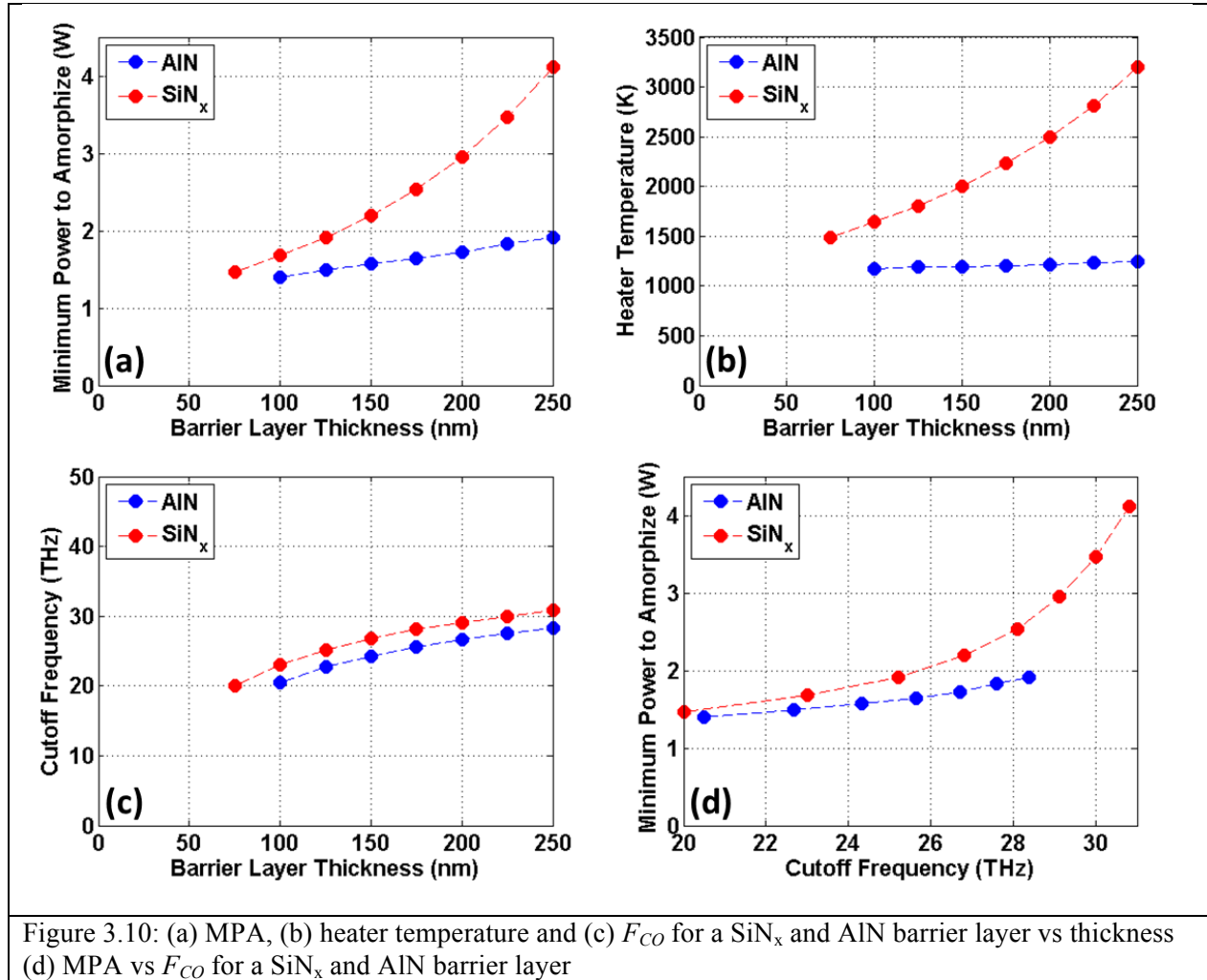


Figure 3.10: (a) MPA, (b) heater temperature and (c) F_{CO} for a SiN_x and AlN barrier layer vs thickness (d) MPA vs F_{CO} for a SiN_x and AlN barrier layer

The MPA for a switch with SiN_x is always higher than that of AlN for a given barrier layer thickness (fig. 3.10(a)). The rate at which the MPA increases with barrier layer thickness is also much higher for SiN_x than for AlN. It is so much higher that, in fact, the MPA for only 125 nm of SiN_x is equal to 250 nm of AlN. The heater temperature is also always much higher for a SiN_x barrier (fig 10(b)). The heater temperature with an AlN barrier layer is between 1170 K (100 nm) and 1250 K (250 nm) while being almost 1500 K for only a 75 nm thick SiN_x barrier. At a SiN_x thickness of 150 nm, the heater temperature is over 2000 K, thereby putting the durability of the heater in question. Due to the lower relative permittivity of SiN_x , the F_{CO} is slightly higher for switches with SiN_x (fig. 3.10(c)). However, an AlN barrier layer requires a lower MPA for a given F_{CO} than does SiN_x (fig. 3.10(d)). This reduction in MPA and heater temperature shows why the use of AlN as the barrier layer is a significant advancement in switch performance.

3.7 Low Resistivity GeTe

The resistivity of the PC-material is a dominant factor in the ON-state resistance of the switch. Previous work has shown the resistivity of sputtered GeTe films ranging from 3 to 4 $\mu\Omega\text{-m}$ [15], [29], [44]. However, Bahal and Chopra [28] showed a resistivity of 1.53 $\mu\Omega\text{-m}$ for a 589 nm thick GeTe film deposited at 250 °C. Reducing the resistivity of GeTe to this level in the switch could double the FCO of the switch without increasing its MPA.

There are two main factors that can affect the resistivity of the GeTe: composition and deposition temperature. A coarse study of the effect of composition on the resistivity GeTe has shown that a 50/50 composition has the lowest resistivity [63]. Sputtering a film from a 50/50 alloyed target does not necessarily result in a film that is also 50/50. This is because the sputter yield of Ge and Te are very different as are their vapor pressures. The lowest achieved resistivity sputter from a 50/50 alloy target was 3.09 $\mu\Omega\text{-m}$. However, once the deposition of the film was completed using co-deposition of

elemental Ge and Te targets, lower resistivities were achieved. The use of co-deposition allowed for the composition of the sputtered films to be slightly varied until the lowest resistivity film was found.

To find the most desirable sputtering conditions, GeTe films were sputtered on Si samples with 1 μm of thermal oxide. The sheet resistance was measured using a 4-point probe. The thickness of the best films of each composition was measured after using an AFM to determine the resistivity of the film. The Te target was deposited using RF magnetron sputtering at a constant 25 W, while the Ge target was deposited using DC magnetron sputtering with power that varied from 35 W to 50 W. The sputtering time was held constant at 1000 seconds thereby making the films different thicknesses. The sputtering gas used was Ar at 60 sccm and 3 mTorr for all the films. The deposition temperature started at 250 $^{\circ}\text{C}$ and was lowered until the sheet resistance of the film was minimized for a given Ge deposition power. The composition of the film was determined using the crystal monitor to measure the rates of Ge and Te individually. Because this is measured at room temperature, it could only be used to determine the composition of the sputtered flux hitting the sample. When the sample is heated, the actual amount of Te that is deposited may be less than what the rate monitor suggests due to its low vapor pressure. This would result in the rate monitor overestimating the Te composition in the sputtered film.

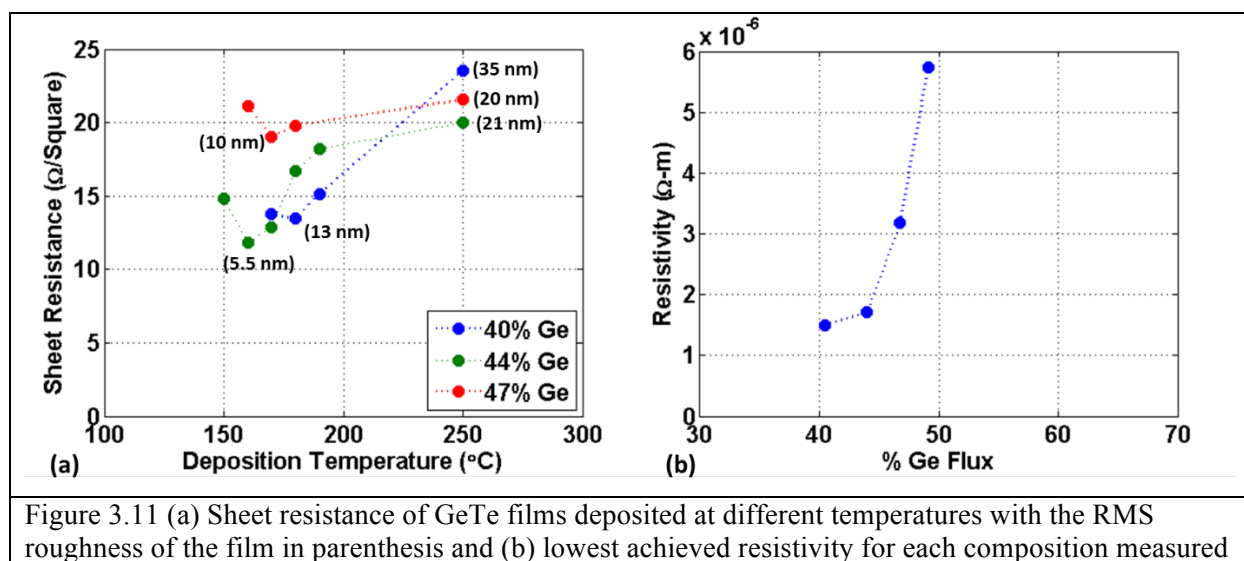


Figure 3.11(a) shows the effect of deposition temperature on sheet resistance for 3 different film compositions. The RMS surface roughness of some of the films is noted in parentheses. The films deposited at 250 $^{\circ}\text{C}$ had the highest sheet resistance as well as RMS roughness. As the deposition temperature is reduced, the sheet resistance also lowers. Both the RMS roughness and the thickness of the film are also dependent on temperature. At a higher deposition temperature, the RMS roughness of the film is higher and its roughness can be seen optically. The average thickness of the film is also higher for those deposited at higher temperatures but the reason for this is not fully understood. This shows that deposition temperature significantly affects the resistivity of the sputtered film. To achieve the best resistivity, the lowest deposition temperature that produces a fully crystalline and smooth GeTe film is desired. Going above that temperature only degrades resistivity. Figure 3.11(b) shows the lowest resistivity for each composition deposited. A resistivity of 1.5 $\mu\Omega\cdot\text{m}$ was achieved for a 40/60 GeTe film and is comparable to the bulk resistivity [28]. However, this composition is based on the crystal monitor. The percentage of Ge in the film is most likely between 45% and 48% due to the evaporation of Te off the substrate during deposition. Secondary ion mass spectrometry (SIMS) could be used to more accurately determine the true composition of the film.

3.8 GeTe Contact Resistance

The contact resistance between the GeTe and contact metallization can become a dominant contributor to the ON-state resistance of the switch if proper precautions are not taken. The choice of contact metal between the GeTe and Au is important in order to prevent the formation of a Schottky contact. The GeTe is a p-type semiconductor [28] and using a metal with a large work function is ideal. Using Pt as the contact metal would be optimal (5.65 eV [64]); however, there is the possibility that it would react with Ge in the PC-material, especially given the high temperatures that are reached during switching [65]. Chua et. al., measured the barrier height for GeTe/metal interface for Al, W, and Ni [66]. He stated that an ohmic contact can be made with crystalline GeTe using metals whose work function is as low as Al (4.28 eV [64]). In another work, he reports the specific contact resistance (ρ_c) of GeTe/W to be $1.40 \Omega\text{-}\mu\text{m}^2$ [67] when the interface is pre-cleaned using a sputter etch. Having a pristine interface between the GeTe and W is critical to minimizing the contact resistance. The notched switch in this case has an advantage because the GeTe, W and Au are all sputtered, one immediately after another, without breaking vacuum. However, in the standard switches process flow, the GeTe is exposed to the atmosphere before the contact metallization is deposited resulting in oxidation of the GeTe surface. In this work, a 3 minute sputter etch at 50 W of RF power is used to clean the surface of the GeTe before the W/Au metallization is deposited.

Using the transfer line method, the sheet resistance (R_{sh}), contact resistance (R_c) and transfer length (L_T) were measured on a 100 nm thick GeTe film. The structure measured was a 20 μm wide strip of GeTe with the space between contacts ranging from 0.5 to 8 squares in length (fig. 3.12(a)). A 4-wire I-V sweep was made between adjacent contacts and the resistance was plotted against the number squares between the contacts (fig. 3.12(b)). From the slope of the line, the sheet resistance is calculated to be $16.8 \Omega/\square$, resulting in a resistivity of $1.68 \mu\Omega\text{-m}$. The y-intercept is equal to $2xR_c$, where R_c is equal to 0.11Ω . The x-intercept is equal to $2xL_T$, where L_T is equal to $0.066 \square$ or $0.131 \mu\text{m}$. The specific contact resistance, ρ_c , is $0.29 \Omega\text{-}\mu\text{m}^2$ and can be calculated using eq. 3.1. The measured ρ_c in this work

($0.29 \, \Omega \, \mu\text{m}^2$) is lower than that seen in Chua et. al. ($1.40 \, \Omega\text{-}\mu\text{m}^2$ [67]). This is most likely due to a more effective sputter etch.

$$\rho_c = R_{sh} L_T^2 \quad (3.1)$$

Using a three-minute sputter etch, the contact resistance for a $20 \, \mu\text{m}$ wide switch is only $0.22 \, \Omega$.

Annealing the contacts may also further reduce the contact resistance [67], [68].

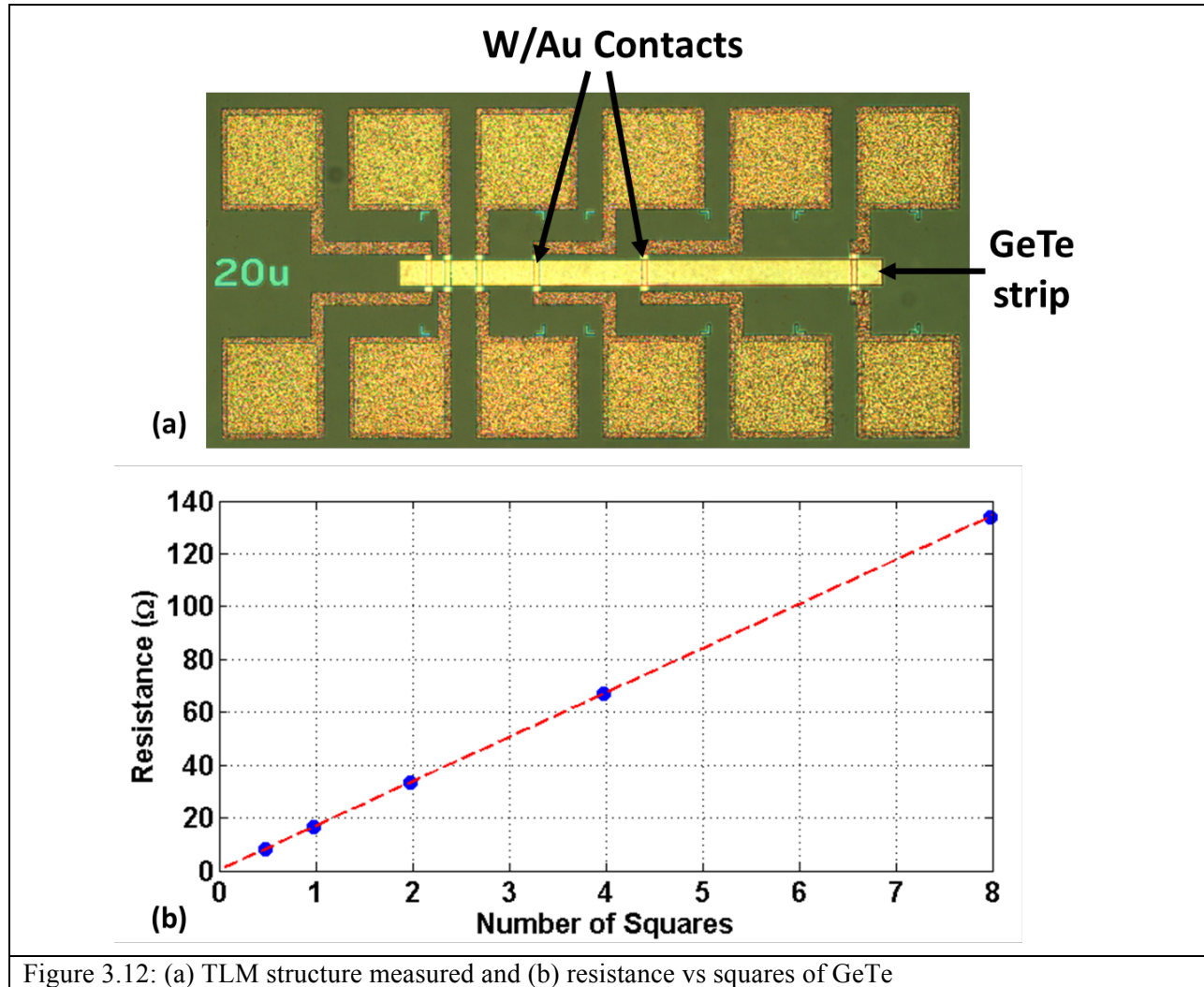


Figure 3.12: (a) TLM structure measured and (b) resistance vs squares of GeTe

3.9 Summary

This chapter details the process flow used to fabricate a standard switch and a notched switch. The standard switch design requires a thorough sputter etch to remove any oxidation on the surface of the GeTe to reduce contact resistance before the contact metal is deposited. The notched switch does not require this but instead requires 100 nm wide notch to be patterned using e-beam lithography and etched into the GeTe.

This work presents three major advancements in the materials used in the switch compared to prior works: W heaters, AlN barrier layer and low resistivity GeTe. A low resistivity W film was developed by depositing at 850 °C. This allows for a significant reduction in voltage and power required to amorphize the switch. Even when the deposition temperature of the W is reduced below the maximum post-processing temperature allowed for a CMOS wafer, a significant reduction in resistivity is still obtained. This allows for the possibility of building a switch directly on a CMOS wafer. By making the heater layer thicker and the switch narrower, it would be possible to reduce the heater resistance to a low enough value that it can be driven by 3.3 V.

The use of AlN as the barrier layer significantly increases the F_{CO}/MPA ratio of the switch. The heater temperature required to melt the PC-material in the RF gap is significantly reduced and would result in greater heater durability.

Using co-deposition of elemental Ge and Te targets, the resistivity of GeTe was reduced by half and would result in up to a 2x gain in F_{CO} . Depositing the film at minimum temperature needed to fully crystallize the GeTe is required to achieve a smooth low resistivity film. When all three advancements are combined, the F_{CO}/MPA ratio doubles from 7.8 THz/W to 15.6 THz/W when simulating a standard switch. The addition of a 100 nm deep notch only increases the F_{CO}/MPA ratio further to 21.1 THz/W.

Chapter 4: DC Switch Characterization

4.1 Abstract

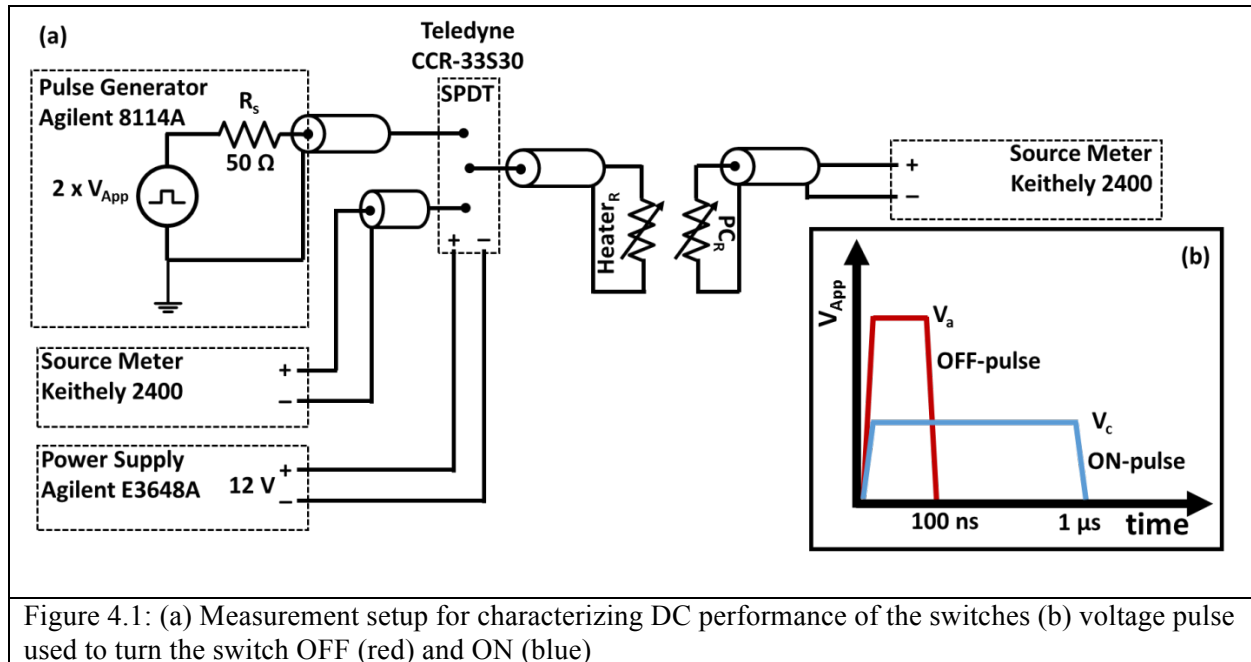
This chapter demonstrates 4-terminal RF PC switches using an AlN barrier layer to electrically isolate a high conductivity W heater. DC testing was done to determine the ON-state resistance (R_{ON}) as well as the minimum power needed to amorphize (MPA) the GeTe. The effects of varying switch dimensions (AlN thickness, GeTe thickness, RF gap length, heater width and switch width) on both R_{ON} and MPA are measured. Increasing the AlN thickness from 105 nm to 200 nm results in only a 14% increase in MPA. Increasing the GeTe thickness from 50 nm to 100 nm results in a reduction in initial R_{ON} from 1.4 Ω down to 1 Ω without increasing MPA. Reducing the RF gap length also significantly reduces R_{ON} from 3 Ω for a 900 nm long RF gap to 1.4 Ω for a 400 nm long RF gap while only increasing the MPA from 1.5 W to 1.8 W.

4.2 Introduction

The fabricated 4-terminal inline RF PC switches went through a series of DC and RF measurements to quantify their performance. This chapter will discuss the DC testing setup and procedure used to measure the minimum power to amorphize (MPA) and the minimum power to crystalize (MPC) for four sets of fabricated switches. The next chapter will discuss the RF measurements. The four sets of switches fabricated varied GeTe and AlN thicknesses as well as the dimensions of the RF gap, switch width and heater width.

4.3 DC measurement Test Setup

Fig. 4.1 shows the DC testing setup. To measure the state of the system, first the resistance of the switch is measured using a Keithely 2400 source meter. An IV sweep is conducted across the device by sourcing current and measuring voltage. The slope of the IV sweep is then used to determine the resistance of the switch. When the switch is in the ON-state, the current is swept from $-100\ \mu\text{A}$ to $100\ \mu\text{A}$ and, for the OFF-state, is swept from $-100\ \text{nA}$ to $100\ \text{nA}$ with a voltage compliance of $100\ \text{mV}$. The heater resistance is then measured by applying $12\ \text{V}$ from the Agilent E3648A power supply to the SPDT switch, followed by an IV sweep from $-1\ \text{mA}$ to $1\ \text{mA}$ with a $100\ \text{mV}$ compliance. Because the as-fabricated device is in the ON-state, the MPA is first measured for the switch. This is accomplished by first measuring the initial state of the system and then, using an Agilent 8114A, a $100\ \text{ns}$ long voltage pulse (10 ns rise/fall time) is sent to the heater. After the voltage pulse is sent to the heater, the state of the system is measured to determine the resistance of the switch and heater. Increasing voltage pulses (in $0.1\ \text{V}$ increments) are sent to the heater until the measured resistance of the switch is above the $10\ \text{k}\Omega$. The MPA is then calculated (as shown in *eq. 4.1*) using the voltage that turned the off switch (V_{App}) and



the corresponding heater resistance (R_H).

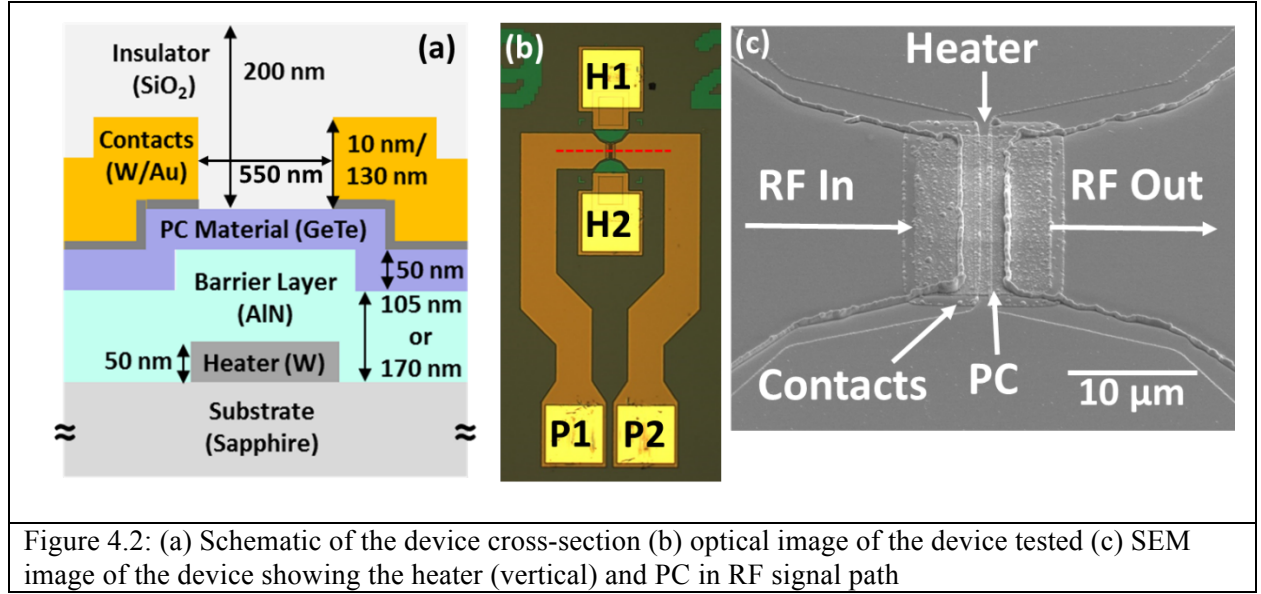
$$Power = \frac{(V_{App} (1 + \frac{R_H - 50}{R_H + 50}))^2}{R_H} \quad (4.1)$$

Once the MPA is found, the same protocol is used to determine the MPC. Increasing 1 μ s long voltage pulses (in 0.1 V increments) are applied to the heater until the switch resistance is within 20% of the initial R of the switch. From there, all cycling and single pulses are applied 0.1-0.2 V above the MPA and MPC voltages, resulting in about a 5% increase in power.

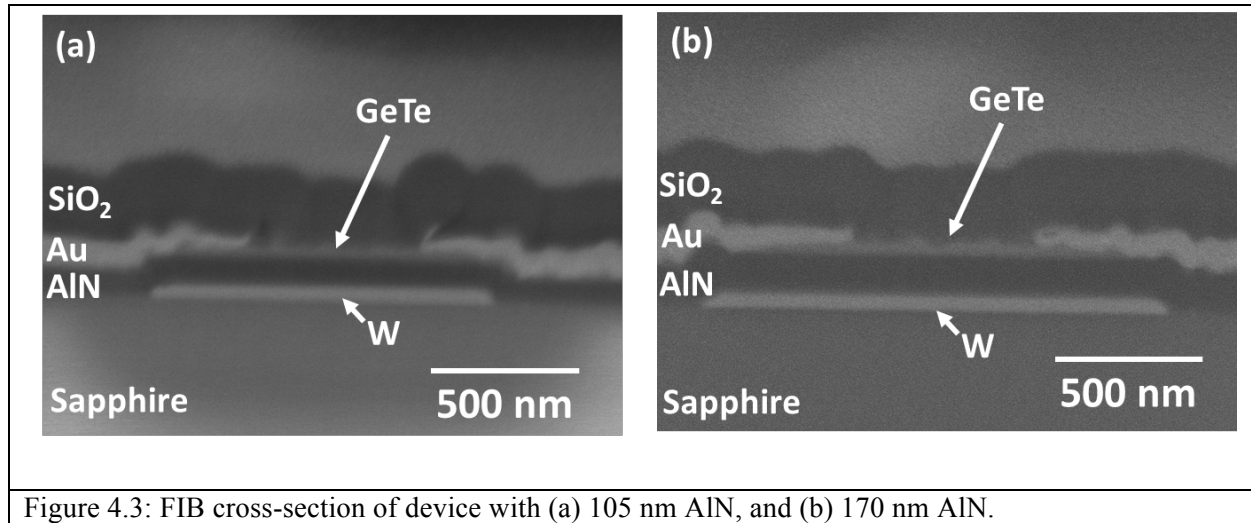
4.4 AlN Thickness Study, 105 nm vs. 170 nm

4.4.1 Switches Fabricated

The first set of switches that will be discussed were used to determine the effect of AlN thickness on the switch on MPA and OFF-state capacitance (C_{off}). Two samples were fabricated that contained over 250 switches each, with one sample using barrier layer thicknesses of 105 nm and the other of 170 nm (fig. 4.2(a)). These were some of the first samples fabricated and the GeTe was sputtered from a single 50/50 alloyed target using DC magnetron sputtering at 250 °C, resulting in a GeTe resistivity of 3.09 $\mu\Omega$ -m. Instead of electroplating 2 μ m of Cu, the traces and pads were patterned using a sputter lift-off of 10 nm W and a 130 nm of Au bi-layer.

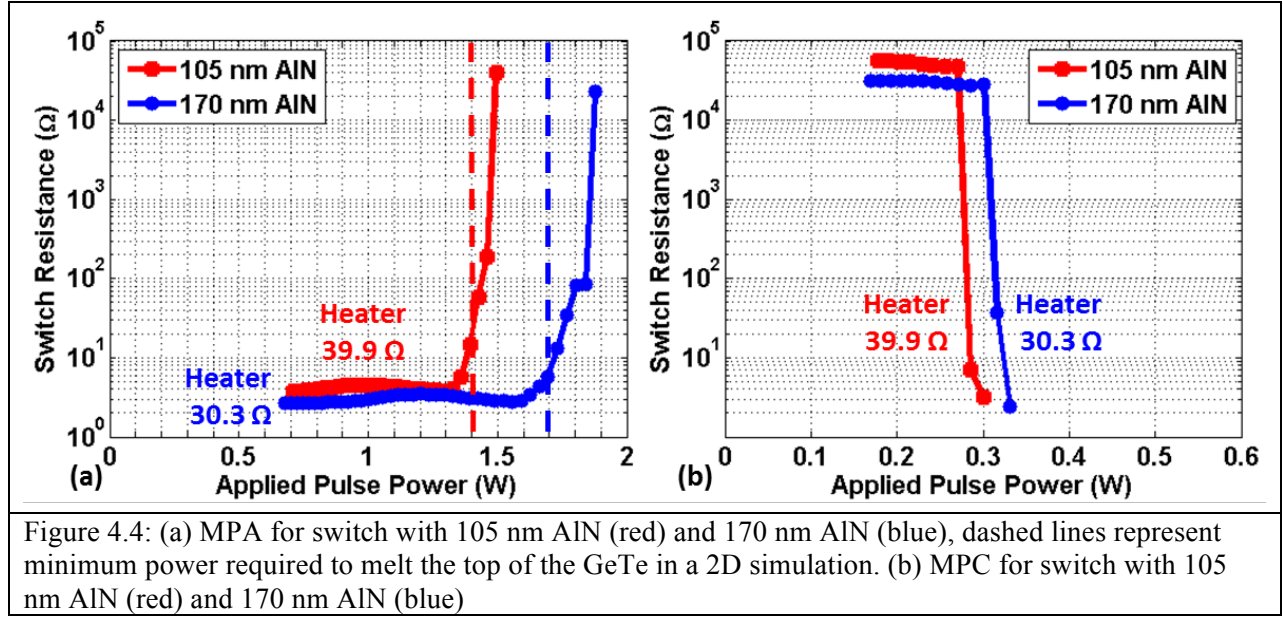


The DC characteristics (ON/OFF state resistance) of the switches were measured across P1 and P2 (fig. 4.2(b)). The transformation was induced by pulsing the heater across H1 and H2 (fig. 4.2(b)). A switch on each sample was measured, where its initial R_{ON} was $2\ \Omega$, to ensure the two switches had similar RF gap lengths. From the FIB cross-section of the devices (fig. 4.3), the RF gaps for both switches were 550 nm long. However, the resistance of the heaters varied between the two switches from $39.9\ \Omega$ for the switch with 105 nm of AlN down to $30.3\ \Omega$ for the switch with 170 nm of AlN. This reduction in heater resistance is due to an increase in heater width which can also be seen in the FIB cross-section of the devices. The heater is $1.06\ \mu\text{m}$ wide for the 105 nm thick AlN (fig. 4.3(a)) and $1.48\ \mu\text{m}$ wide for the 170 nm thick AlN (fig 4.3(b)). Contact photolithography was used to pattern the $1\ \mu\text{m}$ wide heaters. This was at the lower limit of resolution for the contact aligner, and as a result, there can be a high degree of variability in the resulting feature size.



4.4.1 MPA and MPC

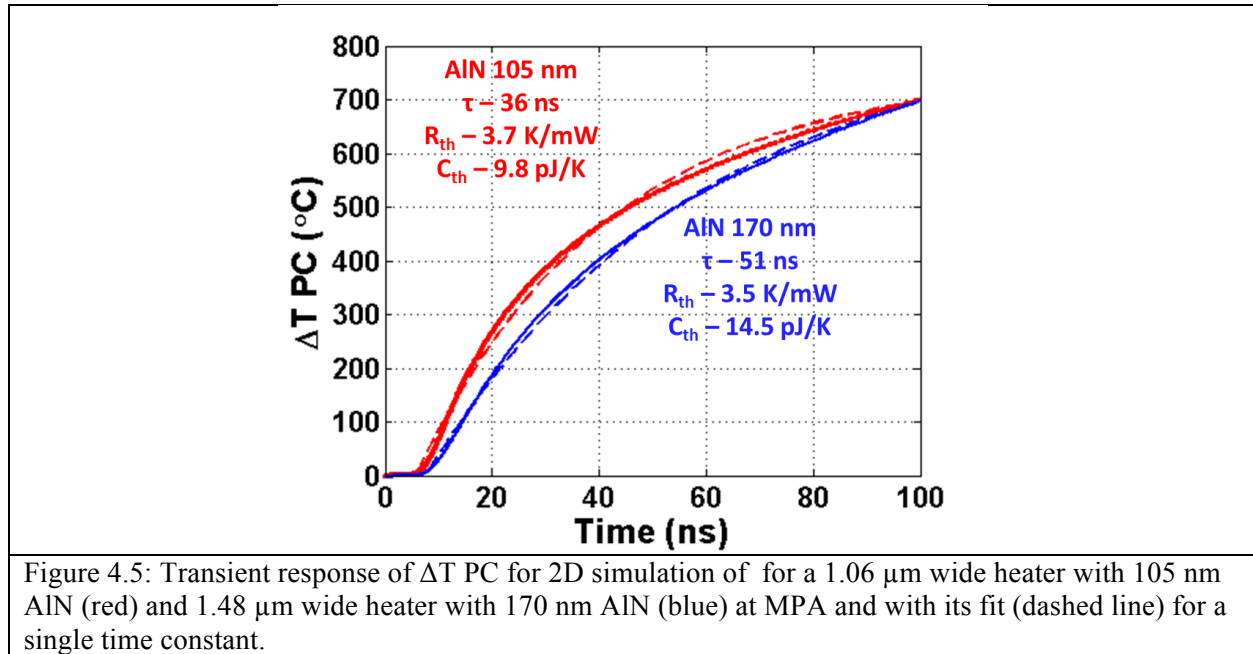
The MPA and MPC results for the two switches can be seen in fig. 4.4. Typically, higher power is needed to switch devices with thicker barrier dielectrics as shown in Chapter 2. However, the increase in power seen in fig. 4.4(a) (1.5 W for 105 nm thick AlN vs 1.9 W for 170 nm thick AlN) is in part due to unintended differences in heater width. An increase in heater width will also lead to an increase in MPA, as shown in Chapter 2. A 2D COMSOL Multiphysics simulation was used to determine the effect of increased heater width on MPA for the measured devices. The dashed red and blue lines in fig. 4.4(a) represent the power required to melt the top of the GeTe in the 2D simulation for 105 nm and 170 nm of AlN, respectively.



4.4.2 Differentiation between AlN thickness and Heater Width on MPA

Four 2D models were built to determine the individual contributions of heater width and AlN thickness on the MPA of the switches. The four models built are as follows: 1.06 μm wide heater with 105 nm AlN, 1.48 μm wide heater with 105 nm AlN, 1.06 μm wide heater with 170 nm AlN and 1.48 μm wide heater with 170 nm AlN. A transient simulation over 10 ms (to ensure the system was at steady-state) with constant heater power was simulated to determine R_{Th} (ΔT of the PC divided by heater power). Next, a 100 ns long pulse was simulated for the four cases at the MPA power. Fig. 4.5 shows the transient response of ΔT PC for a 1.06 μm wide heater with 105 nm AlN (red) and 1.48 μm wide heater with 170 nm AlN (blue). Both transient responses were fitted (dashed line) for a single time constant (τ). It becomes obvious that the increase in power is needed to compensate for the increase in τ . However, the increase in τ is not due to an increase in R_{Th} , but instead an increase in the thermal capacitance (C_{Th}). Based on the simulations, it can be concluded that of the 22% total increase in simulated power (1.4 vs 1.7 W) required to melt the GeTe with thicker AlN, less than half of the increase (0.11 W or a 8% net effect) can be attributed to the increased heater width and its requirement of more power to achieve the same temperature. The remaining increase in required power (0.19 W or a 14% net effect) is due to the

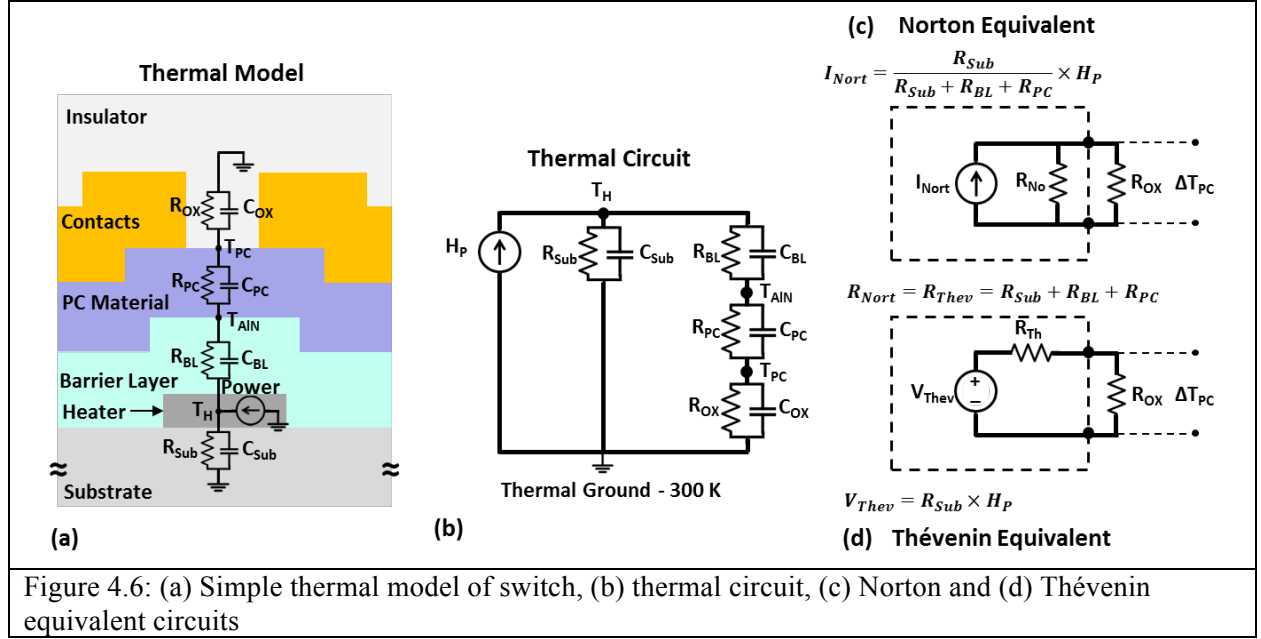
thicker AlN. This increase in required power can be attributed to both changes in thermal resistance (R_{Th}) and thermal capacitance (C_{Th}) introduced by the AlN. Simulations show an increase in the switch C_{Th} of 13% due to the increase in AlN thickness. The thicker AlN also lowers the thermal resistance of the heater to thermal ground by 10%, which necessitates more power. However, the efficiency of thermal coupling between the heater and the phase change element only decreases by 2%. Thus, the contribution to increased MPA from thicker AlN is equally divided between thermal conduction and thermal capacitance under these transient pulse conditions. However, it is the heat spreading facility of the thicker AlN that dominates the conduction effects. This is consistent with the effect of a high thermal conductivity layer.



4.4.3 Thermal Model of Switch

The mechanism for an increase in C_{Th} and a decrease in R_{Th} , when the thermal impedance due to the AlN must increase with thickness, is not straightforward. A simple thermal model can be made of the switch (fig. 4.6(a)), using a single R_{Th} and C_{Th} for each layer in the switch, and the power in the heater can be modeled as a current source. When the model is transformed into a circuit (fig. 4.6(b)), the current

source (Heater Power (H_P)) is in parallel with the thermal impedance of the substrate as well as the series combination with the material on top of the heater. The C_{Th} for all the layers increases with heater width due to a larger volume being heated.



When the AlN barrier layer thickness increases, C_{BL} and R_{BL} both increase. The increase in C_{BL} results in an increase in C_{Th} of the switch and an increase in R_{BL} actually reduces the R_{Th} of the switch. When R_{BL} increases, the temperature of the heater (H_T) increases. However, this increase in H_T does not result in an increase in T_{PC} . This is because the temperature drop across the AlN barrier layer increases due to its larger thermal resistance. Therefore, in order to achieve the T_{PC} required to melt the PC layer, the heater power must increase. This becomes more obvious when the thermal circuit is simplified to its Norton (fig. 4.6(c)) and Thévenin (fig. 4.6(d)) equivalent circuits. The thermal resistance of the oxide (R_{OX}) is the load and the voltage drop across the load (oxide) is the ΔT_{PC} . The Norton (R_{Nort}) and Thévenin (R_{Thev}) equivalent resistance is the series addition of R_{Sub} , R_{BL} , and R_{PC} . As R_{BL} increases, the equivalent resistance also increases. The ΔT_{PC} can be calculated from these variables as shown in eq. 4.2.

$$\Delta T_{PC} = \frac{R_{OX} \times R_{Sub}}{R_{Sub} + R_{BL} + R_{PC} + R_{OX}} \quad (4.2)$$

The power generated in the heater must be increased to maintain ΔT_{PC} when R_{BL} increases. R_{Th} (as shown in eq. 4.3) can then be derived from eq. 4.2.

$$R_{Thermal} = \frac{\Delta T_{PC}}{H_P} = \frac{R_{OX} \times R_{Sub}}{R_{Sub} + R_{BL} + R_{PC} + R_{OX}} \quad (4.3)$$

It now becomes obvious that an increase in R_{BL} results in a decrease in R_{Th} and thus requires more power to turn off the switch.

4.4.4 Cycling Data

Fig. 4.7 presents the cyclability of both switches for 80 pulses, with the heater pulsed using a voltage that was 0.1 V higher than that which is extracted from MPA and MPC measurements (fig. 4.4). This resulted in 2% more power over MPA and 5% more power over MPC. The ON-state resistance held constant for both switches at 2 Ω while the OFF-state resistance remained nearly constant at around 10 k Ω .

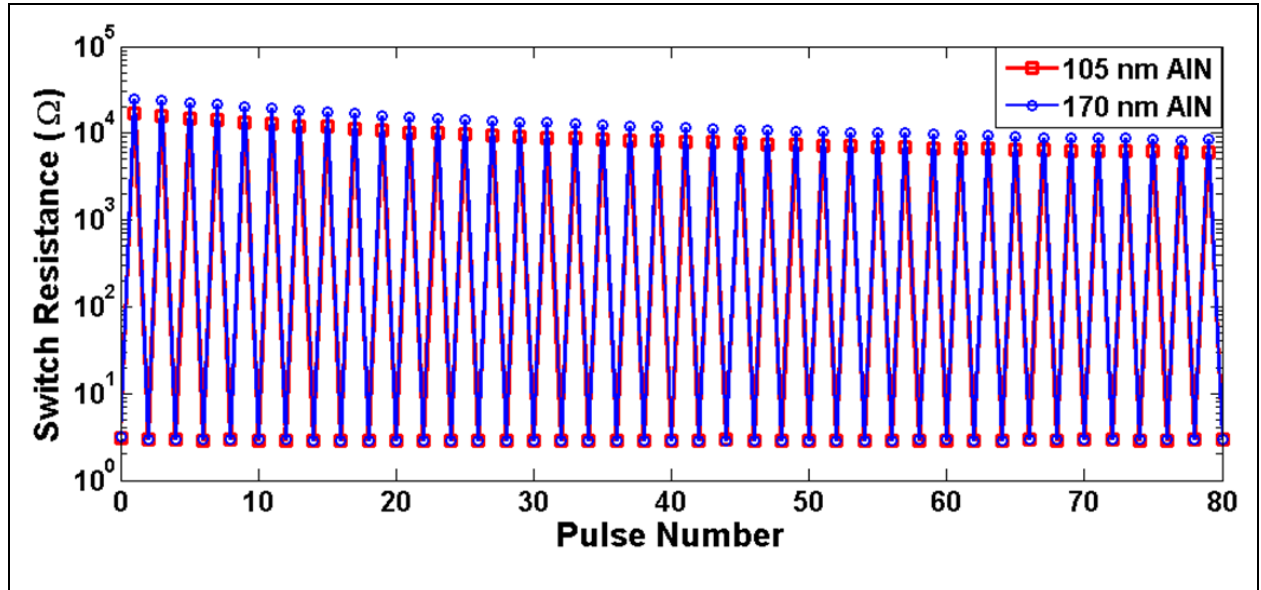
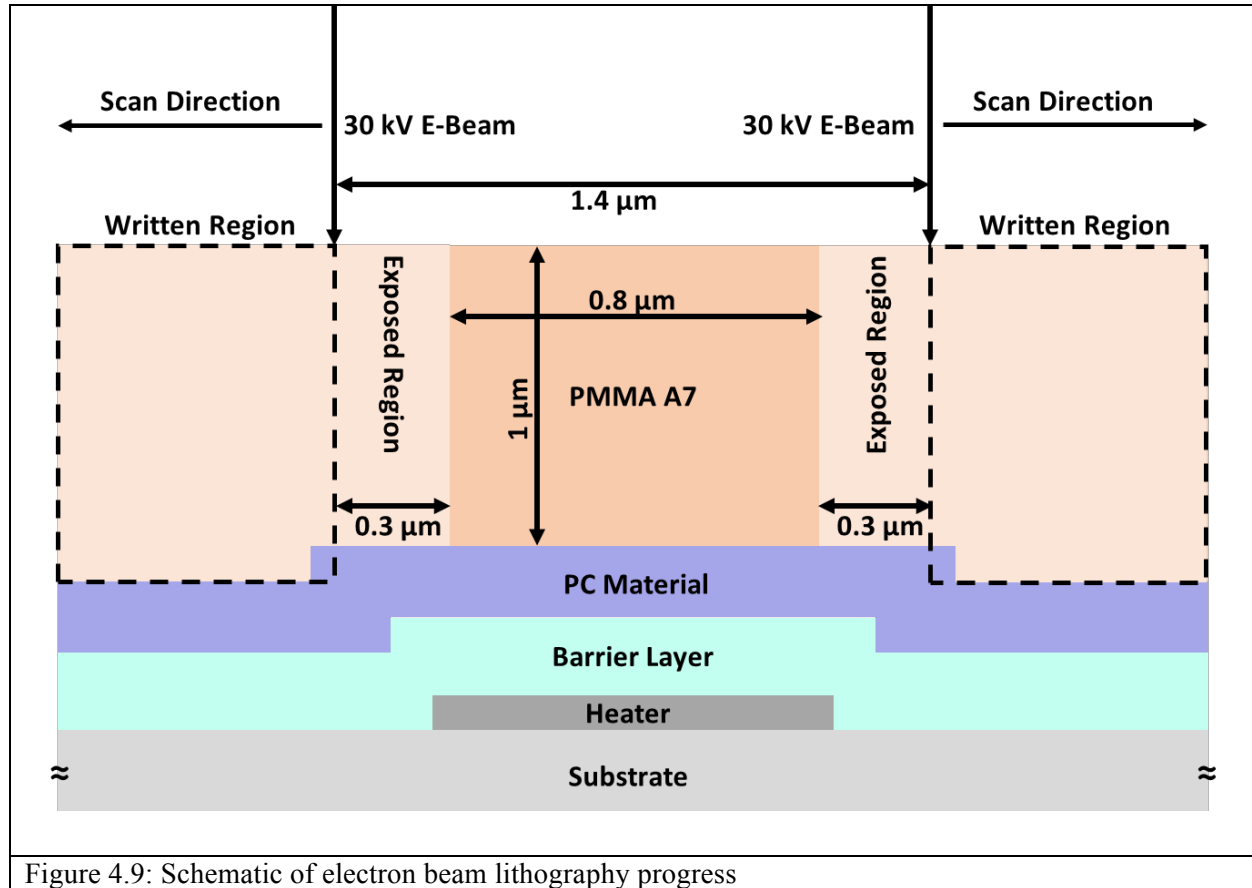


Figure 4.7: Resistance of switch with 105 nm AlN barrier (red) and 170 nm AlN barrier (blue) after pulsing of heater

This results in the RF gap being $0.6\text{ }\mu\text{m}$ smaller than that which is written by the electron beam. To achieve the desired RF gaps for this sample, patterns with gaps ranging from $1.5\text{ }\mu\text{m}$ down to $1.0\text{ }\mu\text{m}$ (in $0.1\text{ }\mu\text{m}$ increments) were written.



4.5.2 MPA and MPC

The MPA (fig. 4.10(a)) and MPC (fig. 4.10(b)) was measured for each RF gap length. The MPA for RF gap lengths above 500 nm remains constant around 1.5 W (fig. 4.10(c)). Not until the RF gap is reduced even further, to 400 nm , does the MPA increase significantly to above 1.8 W . This increase in MPA was also seen for the simulations in Chapter 2; however, the MPA did not significantly increase until the RF gap was 300 nm and below. The premature rise in MPA may be due to incorrect calibration of the RF gap length.

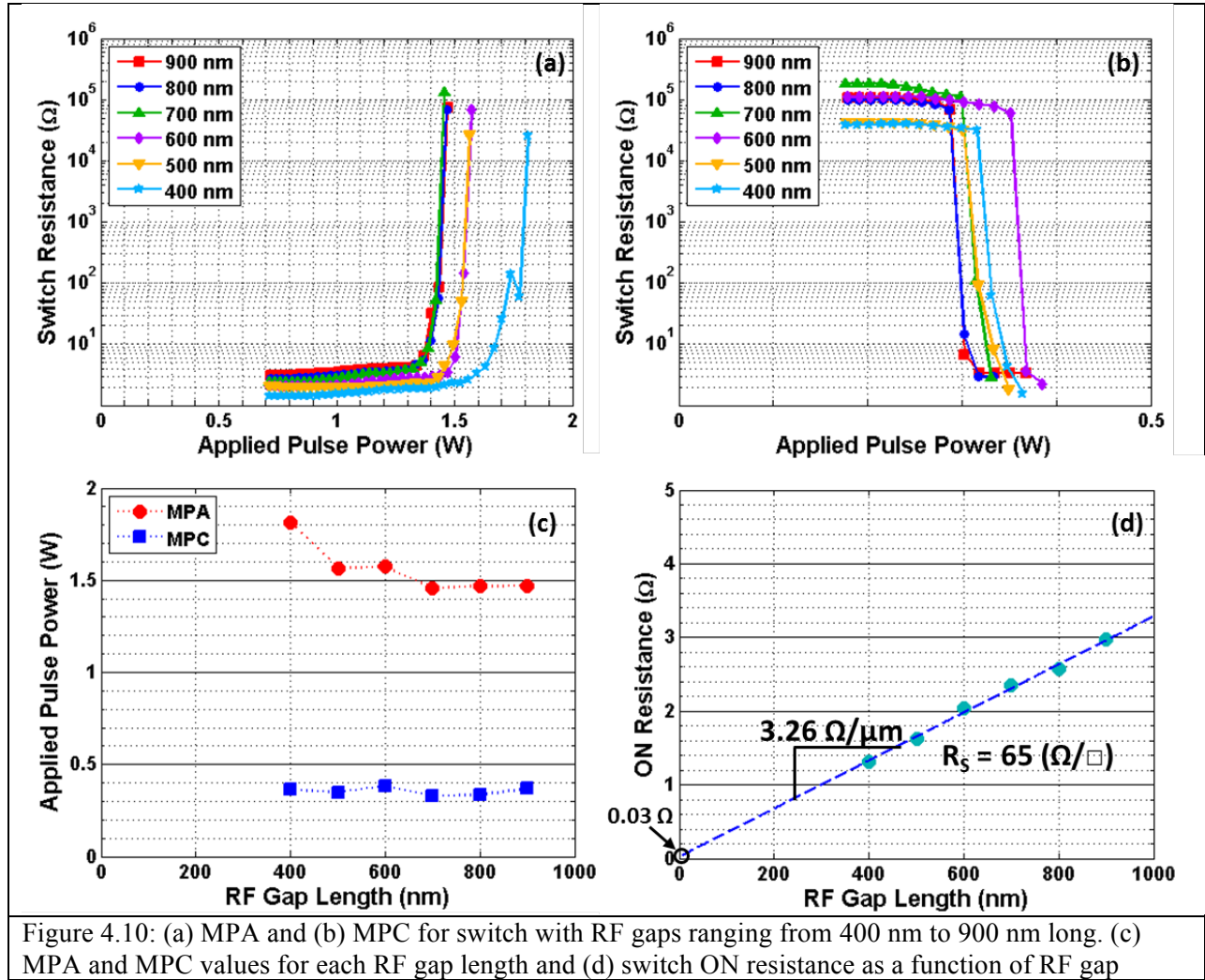


Figure 4.10: (a) MPA and (b) MPC for switch with RF gaps ranging from 400 nm to 900 nm long. (c) MPA and MPC values for each RF gap length and (d) switch ON resistance as a function of RF gap

The ON-state resistance of the switch is plotted against the RF gap length in fig. 4.10(d). The slope of the linear fit is $3.26 \Omega/\mu\text{m}$ for a $20 \mu\text{m}$ wide switch. The contact resistance that results from the fit is 0.03Ω , which is an order of magnitude smaller than what was measured using the TLM structure presented in Chapter 3. However, the extracted sheet resistance from the slope of the fit shows a sheet resistance value of $65 \Omega/\square$, which is almost twice the resistance that was measured on a Van der Pauw structure. The source of this difference is not due to an incorrect calibration of the RF gap length. An incorrect calibration of the RF gap length would only result in the contact resistance that is extracted from the fit being incorrect and would not change the slope (R_s) of the fit. This difference in sheet resistance must be better understood in order to maximize the performance of the switch. This increase in sheet

resistance resulted in an R_{ON} of $1.3\ \Omega$ instead of the $0.76\ \Omega$ that could have been achieved had the sheet resistance been what was measured by the Van der Pauw structure.

4.5.3 Cycling Data

Fig. 4.11(a) presents switch cyclability for 198 pulses (99 cycles), with the heater pulsed using an OFF voltage pulse of 9.2 V (1.7 W) and an ON voltage pulse of 4.4 V (0.38 W). This resulted in 2% more power over MPA and 10% more power over MPC. The OFF-state resistance rose from $25\ \text{k}\Omega$ to over $50\ \text{k}\Omega$ after 99 cycles. The ON-state resistance (fig. 4.11(b)) held constant at as low as $1.65\ \Omega$ over the first 60 cycles but then began to increase. At the end of the 99 cycles, the ON resistance grew to $4.8\ \Omega$.

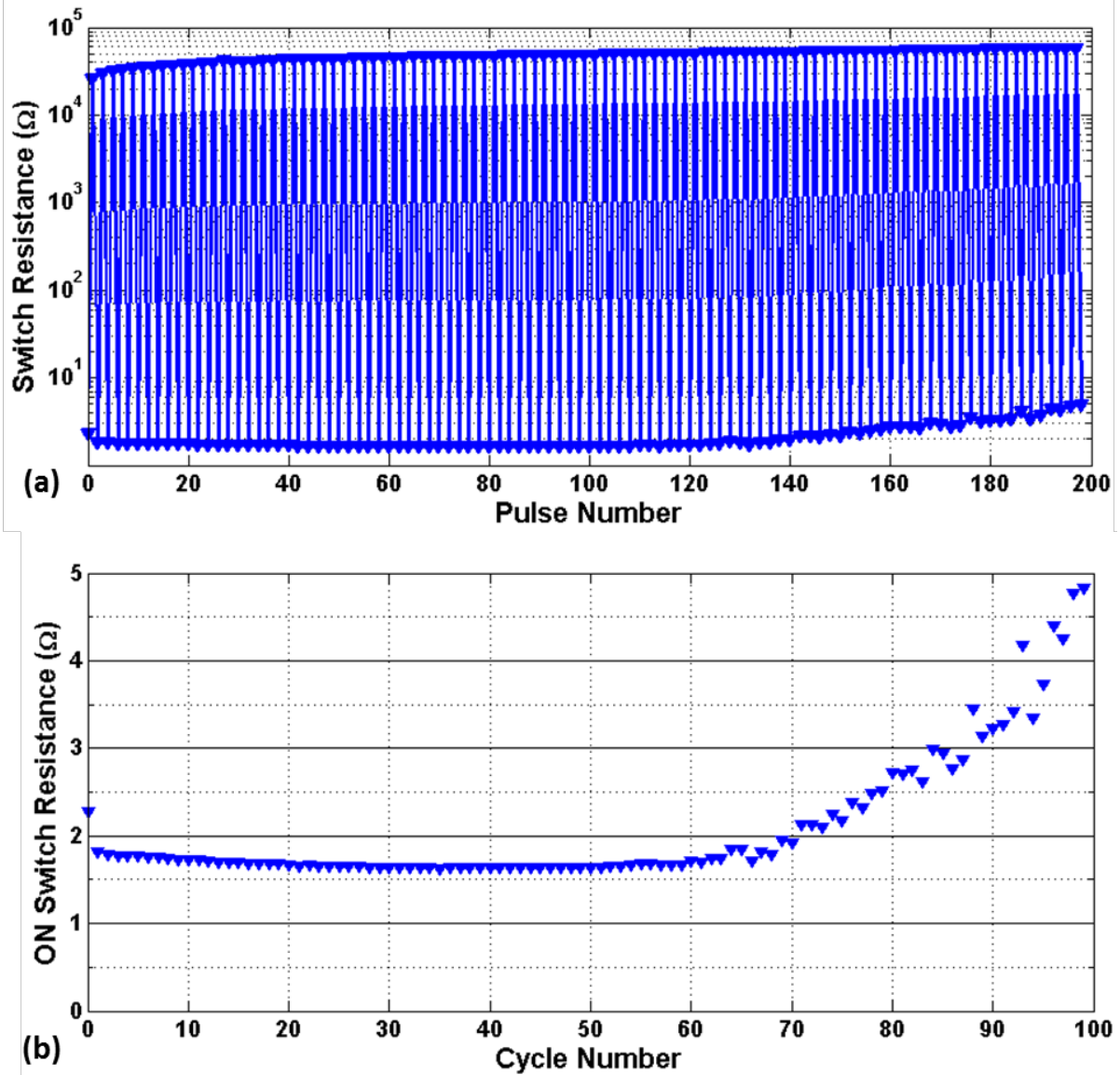


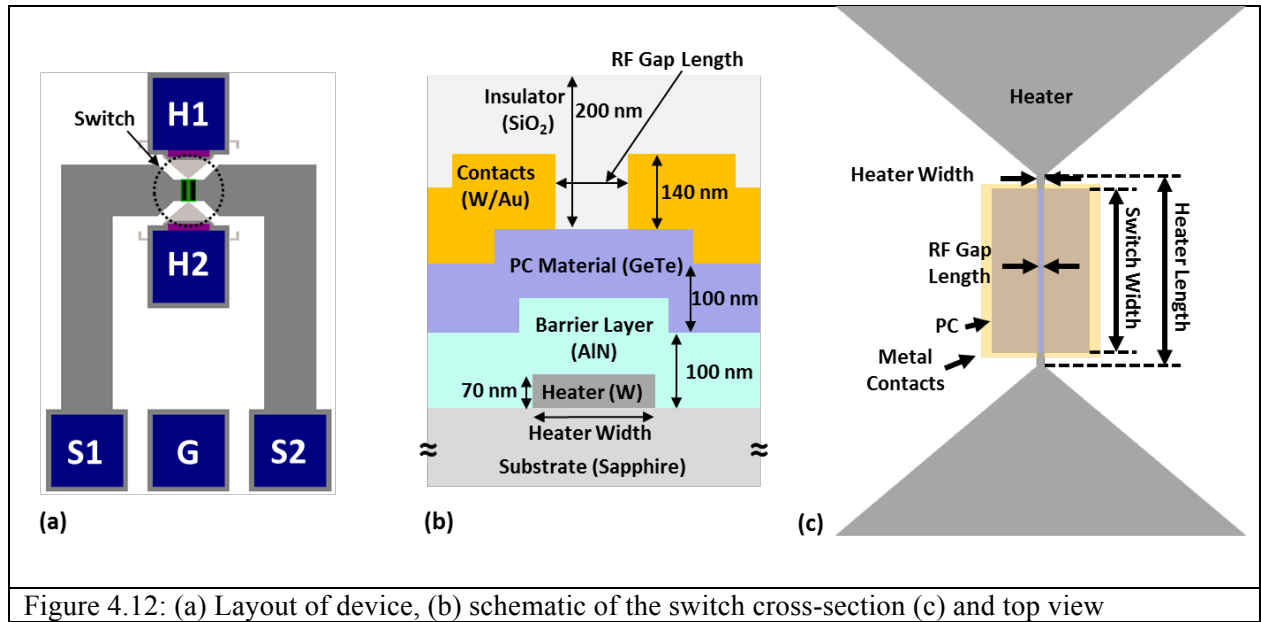
Figure 4.11: (a) Resistance of switch with 500 nm RF gap length after pulsing of heater with (b) corresponding R_{ON} for each cycle

4.6 GeTe 100 nm Thick

4.6.1 Switches Fabricated

The next set of switches that will be discussed were fabricated using 100 nm of GeTe on 100 nm of AlN. The GeTe was sputter etched for the standard 3 minutes before the contact metal was deposited. From the Van der Pauw structure and TLM measurement, the sheet resistance of the GeTe was 17 Ω/\square

($1.7 \mu\Omega\text{-m}$). The contact resistance that resulted from the TLM measurements was 0.22Ω (2 contacts) for a $20 \mu\text{m}$ wide strip of GeTe. This set of devices not only had thicker GeTe but also had a varying range of heater widths, switch widths and RF gaps. The heater widths used were $1, 2$ and $3 \mu\text{m}$ wide. The switch widths used were $10, 20$ and $30 \mu\text{m}$. The RF gap lengths used were $400, 600$ and 800 nm . All combinations of heater widths, switch widths and RF gaps were fabricated resulting in 27 different switch geometries. These different switch geometries allowed for the study of the effect of heater width and switch width on MPA, R_{ON} and C_{OFF} . The resistance of the switch was measured between S1 and S2 (fig. 4.12(a)). The transformation was induced by pulsing the heater across H1 and H2 (fig. 4.12(a)). The schematic of the cross-section and top view of the switch are shown in fig. 4.12(b) and fig. 4.12(c), respectively.



4.6.2 Heater Resistance

The resistances for all of the heaters were measured and plotted versus heater length (fig. 4.13(a)) for each heater width. The heater length is always $3 \mu\text{m}$ longer than the switch width (i.e., a $20 \mu\text{m}$ wide switch has a $23 \mu\text{m}$ long heater). The slope of each line was calculated and its inverse was plotted versus heater width (fig. 4.13(b)). The sheet resistance of the W heater can be calculated by inverting the slope

of the fitted line. The processing bias (how far the dimension of interest, in this case width, varies from what was expected) can also be determined from where the fitted line intercepts the x-axis. The sheet resistance (R_S) for the tungsten heater was $0.9 \Omega/\square$ and the heaters were $0.11 \mu\text{m}$ narrower than what was expected (i.e. a $1 \mu\text{m}$ wide heater was actually $0.89 \mu\text{m}$ wide). It is important to note that the sheet resistance of tungsten film measured using the Van der Pauw structure resulted in R_S of $1.02 \Omega/\square$. This difference in R_S has not been resolved and there are currently no hypotheses that might explain it.

The series resistance leading up to the heater includes the cables, probes and contact pads and can be determined by plotting the resistance of the heater versus the inverse of the corrected heater width (fig. 4.13(c)) for the three different lengths of heaters. The y-intercept of the fit (the series resistance that is not width dependent) is 6.8Ω . The reason for the difference in series resistance seen in fig. 4.13(a) is due to a width dependent series resistance that is present when the heater resistance is plotted versus heater length, but drops out when heater resistance is plotted versus the inverse of heater width. This width dependent series resistance is due to the fan-out region between the heater pads and the heater trace itself, as seen in fig. 4.12(b) (triangle shaped area).

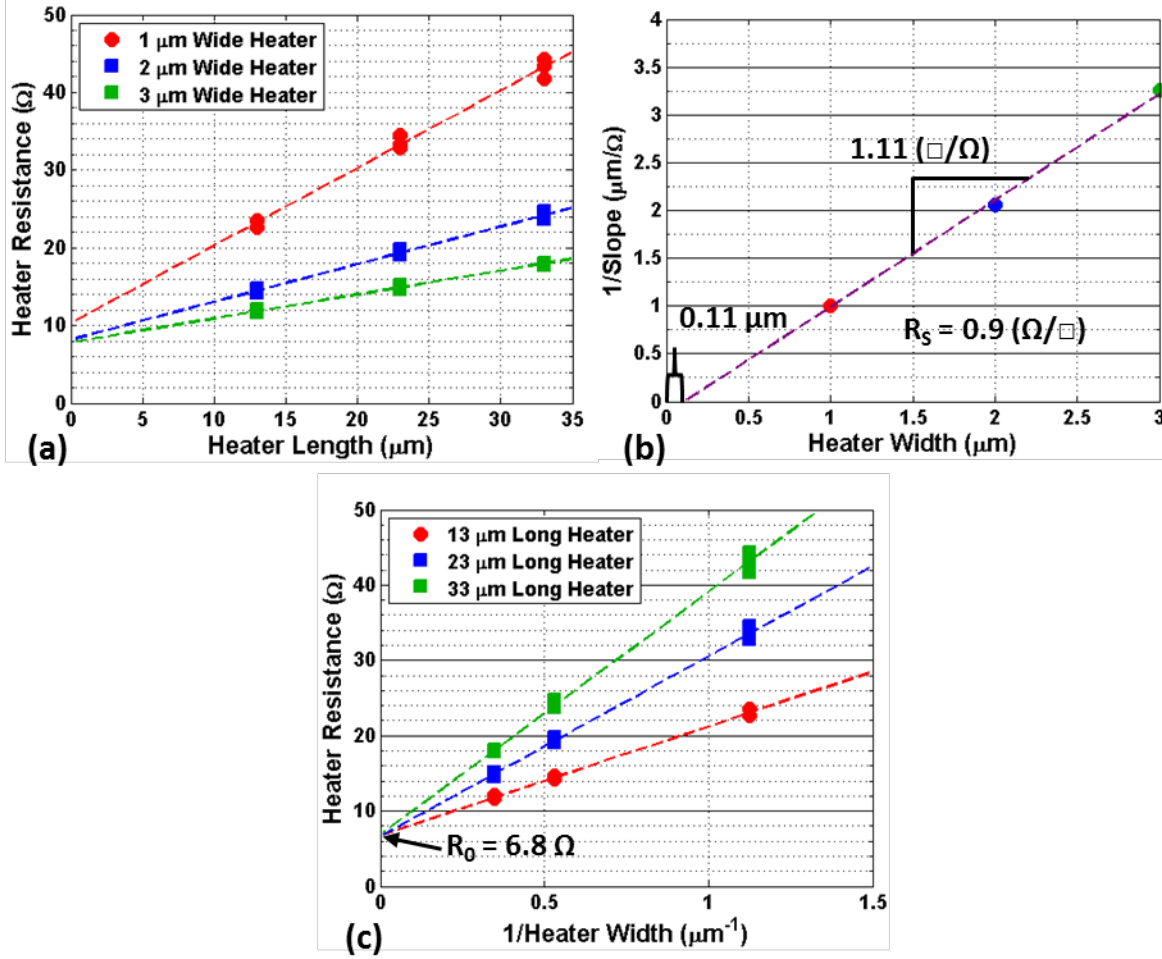


Figure 4.13: (a) Heater resistance versus heater length for 1 μm , 2 μm and 3 μm wide heaters, (b) inverse of heater length slope for each heater width, (c) heater resistance versus the inverse of the corrected heater width for 13 μm , 23 μm and 33 μm long heaters

4.6.3 Initial R_{ON}

A comparison of the initial ON resistance (R_{ON}) is made for all of the varying switch dimensions. It was expected that R_{ON} would scale with RF gap length based on the R_s of the film, as well as with the inverse of the switch width, and that R_{ON} would not change with heater width. However, as seen in fig. 4.14(a), R_{ON} decreases with increasing heater width. The effect is greatest for the longest RF gap of 800 nm and very minimal for the 400 nm long RF gap. This suggests that there is some interaction between heater width and R_s . When R_{ON} for a 20 μm wide switch is plotted versus RF gap length

(fig. 4.14(b)), R_S is over twice as large for the switches with a 1 μm wide heater ($42 \Omega/\square$) than for 2 μm and 3 μm wide heaters ($19 \Omega/\square$). For comparison, R_S measured from the Van der Pauw structure was $17 \Omega/\square$. This increase in sheet resistance in the device as compared to the Van der Pauw structure is similar to that seen in the previous set of devices discussed. There may be a pathological reason for this increase in R_S that is not as severe for switches with wider heaters. The effective contact resistance also decreased for a 1 μm wide heater. For the 2 μm and 3 μm heaters, the contact resistance was about 0.55Ω ; however, for the 1 μm heater, it is 0.13Ω . The contact resistance measured using TLM was 0.22Ω . This difference in contact resistance in the wider heaters may be due to a longer RF gap than that which was expected. For this to be the case, the RF gap would need to be 350 nm longer than that which was expected (i.e. an expected 400 nm long RF gap is in actuality 750 nm long).

The sheet resistance and contact resistance does scale with switch width (fig. 4.14(c)). For switches with a 2 μm wide heater, R_S is $19 \Omega/\square$ and the contact resistance is about $11 \Omega\text{-}\mu\text{m}$ for two contacts. R_{ON} for the three RF gap lengths are plotted versus the inverse of the switch width in fig. 4.14(d). The R_{ON} for the 400 nm long RF gaps lie in a straight line; however, the R_{ON} for the 600 nm and 800 nm long RF gaps are more scattered due to their increased dependence on heater width. To achieve a 1Ω switch, a 20 μm wide switch can be used if the RF gap is 400 nm long or less. If RF gaps above 400 nm are used, the width of the switch must be increased to 30 μm .

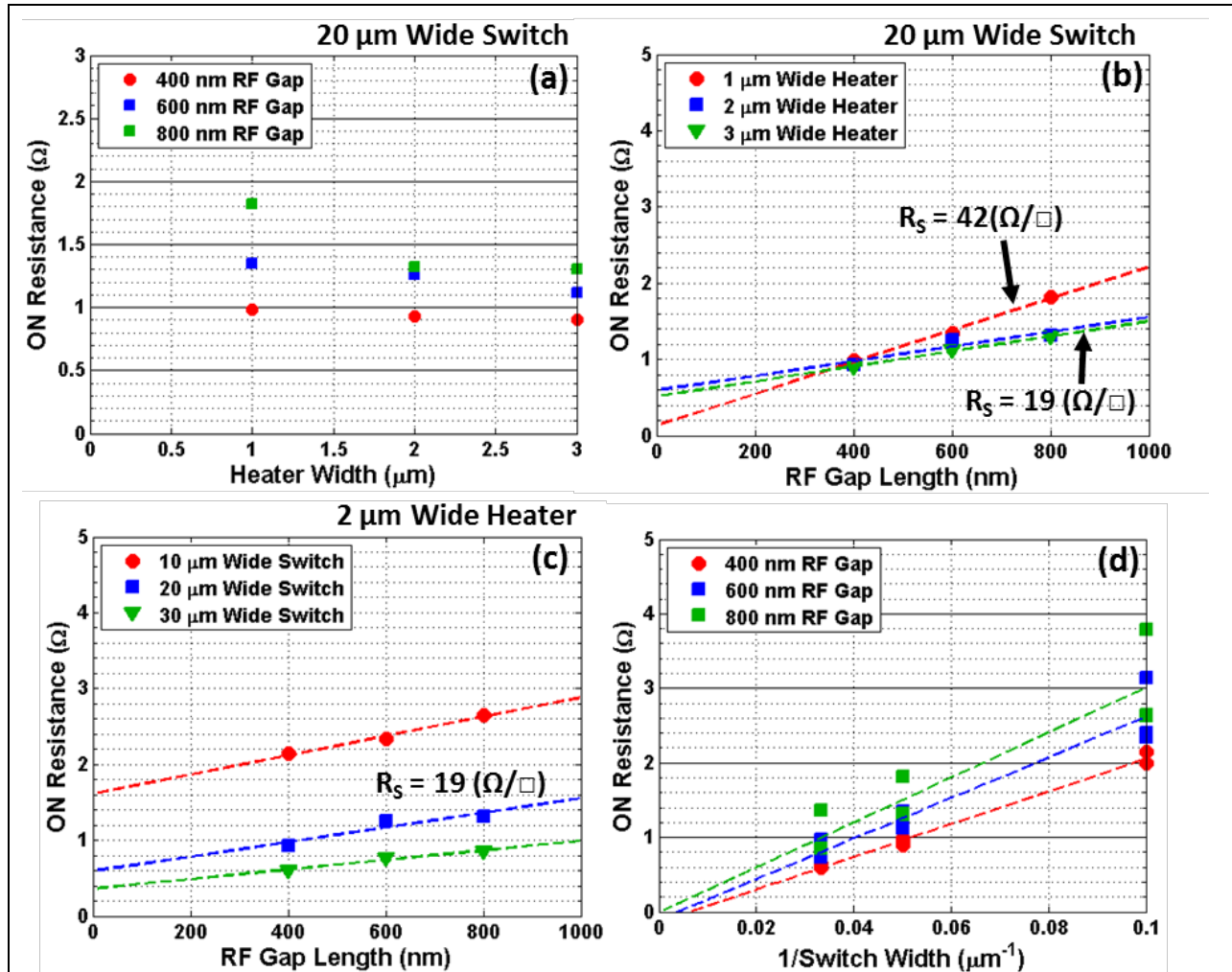


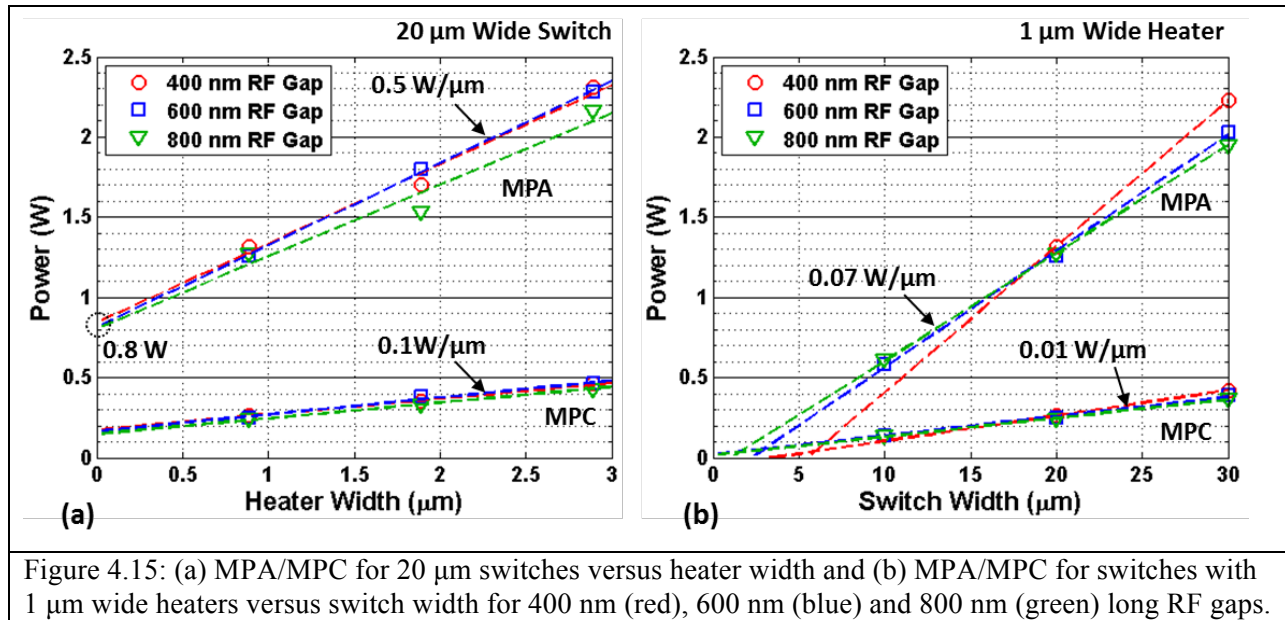
Figure 4.14: (a) Initial switch resistance for a 20 μm switch vs heater width for 400 nm (red), 600 nm (blue) and 800 nm (green) long RF gaps. (b) Initial switch resistance for a 20 μm switch vs RF gap length for 1 μm (red), 2 μm (blue) and 3 μm (green) wide heaters. (c) Initial switch resistance for switches with a 2 μm wide heater vs RF gap length for 10 μm (red), 20 μm (blue) and 30 μm (green) wide switches. (d) Switch resistance versus the inverse of switch width for 400 nm (red), 600 nm (blue) and 800 nm (green) long RF gaps.

4.6.4 MPA and MPC

The MPA and MPC were measured for all of the different combinations of switch dimensions. It is important to note that two combinations of switches had difficulty being turned off. These two switches were 30 μm wide and had a 400 nm long RF gap. The switches with 1 μm and 2 μm wide heaters can only be turned off once before the heater fails.

The MPA and MPC for 20 μm wide switches are plotted versus heater width in fig. 4.15(a).

MPA and MPC are not a strong function of RF gap length but are a strong function of heater width. MPA and MPC increase by 0.5 W and 0.1 W per micron of heater width, respectively. This shows that reducing the heater width is critical to reducing the power requirement of the switch. The MPA, however, could never be below 0.8 W, even with the narrowest of heaters. Increasing the switch width reduces R_{ON} ; however, it results in an increase in MPA and MPC (fig. 4.15(b)). For switches with a 1 μm heater, the MPC increases by 0.01 W per micron of switch width while the MPA increases by 0.07 W per micron of switch width. Therefore, there is a direct trade-off between R_{ON} and MPA. The R_{ON} -MPA product is minimized for 20 μm wide switches. A 20 μm wide switch with a 1 μm wide heater and 400 nm long RF gap has the smallest R_{ON} -MPA product of 1.3 Ω -W.



4.4.5 Parallel Switches

Using devices where two switches and heaters are in parallel was also investigated on this sample (fig. 4.16). Both heaters could be pulsed simultaneously using a GSG probe (Ground-Signal-Ground) across pads H1, H2 and H3, respectively (fig. 4.16). The resistance of the two switches in parallel was measured across pads S1 and S2 (fig. 4.16). The MPA was determined for all of the switch geometries

discussed earlier. However, not all of the switches that worked as a single switch were also successful in parallel. None of the switches with a 1 μm wide heater could be turned off before the heaters failed. Also, only a 3 μm wide heater was able to turn off a 30 μm wide switch with a 400 nm RF gap. For the switches that did work, it would be expected that the R_{ON} -MPA product would also remain the same. However, it was lower for the switches with the parallel heaters. The R_{ON} of the switch was reduced by half, but the MPA did not double. After closer examination, this is due to the fact that the MPA is calculated based on the incidence pulse that arrives at a room temperature heater. However, when the heater increases in temperature, the power dissipated by the heater is different than when it was at room temperature. If the temperature of the heater is corrected for, the MPA for the switches in parallel is indeed twice that of a single switch. Table 4.1 shows the comparison for two 20 μm wide switches, with a 2 μm wide heater for a heater ΔT of 1000 K.

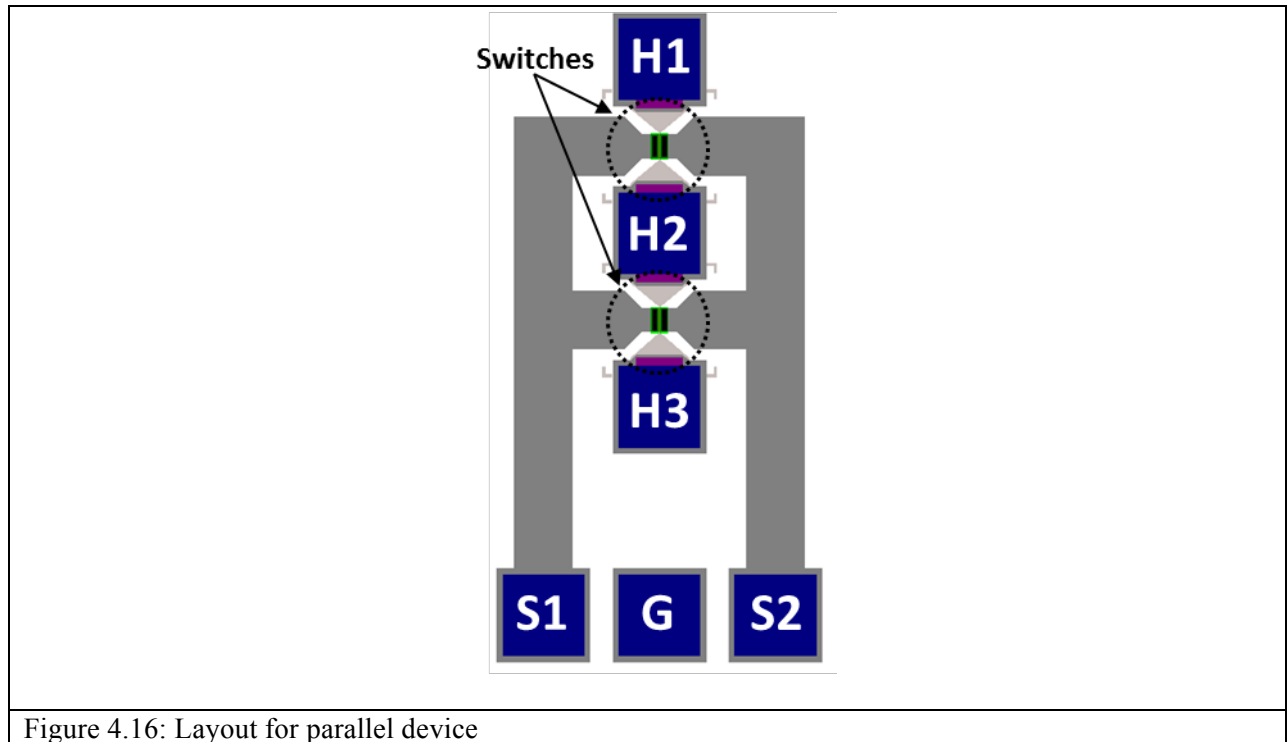


Figure 4.16: Layout for parallel device

	RF Gap (nm)	R_{ON} (Ω)	Heater R (Ω)	V_{App} (V)	MPA (W)	Heater R at Temp (Ω)	V at Temp (V)	Power At Temp (W)
Single	400	0.93	19.2	10.3	1.70	55.5	10.8	2.12
Single	600	1.26	19.1	10.6	1.80	55.1	11.1	2.24
Parallel	400	0.51	8.3	15.8	2.44	26.3	10.9	4.51
Parallel	600	0.65	8.3	15.7	2.41	26.3	10.8	4.45
Table 4.1: Comparison of single switch with parallel switches								

Another application of parallel switches is to split a single 20 μm wide switch into two 10 μm wide switches in parallel. This has the advantage of reducing the voltage required to switch the device off. Table 4.2 shows the comparisons of a single 20 μm wide switch to two 10 μm wide switches in parallel (1 μm wide heater and 800 nm long RF Gap). The applied voltages (V_{App}) from the pulse generator are similar; however, the incident voltage across the heater (V_I) is only 3 V for parallel switches compared to 6.6 V for the single switch. The voltage across the heater for a heater ΔT of 1000 K is also lower for parallel switches. This demonstrates that using parallel switches is an effective way to reduce the voltage required to switch a device.

	R_{ON} (Ω)	Heater R (Ω)	V_{App} (V)	V_I (V)	MPA (W)	Heater R at Temp (Ω)	V at Temp (V)	Power At Temp (W)
1 – 20 μm	1.82	34.5	8.1	6.6	1.27	138.9	11.9	1.02
2 – 10 μm	2.13	10.7	8.4	3.0	0.82	36.6	7.1	1.38
Table 4.2: Comparison of single 20 μm wide switch with two 10 μm wide switches in parallel								

4.7 AlN 200 nm Thick

4.7.1 Switches Fabricated

The last set of switches that will be discussed had 50 nm of GeTe with a 200 nm thick AlN barrier layer. Earlier in the chapter, switches with 105 nm and 170 nm of AlN were discussed. This set of devices was fabricated to see how thick the AlN barrier layer could be while still maintaining functionality. A schematic of the device cross-section can be seen in fig. 4.17. The switches were fabricated with the same 27 combinations of switch widths, heater widths and RF gap lengths as

previously discussed. However, only the switches with the 1 μm wide heater were able to be cycled off before the heater failed. The inability to turn the switches off with wider heaters is most likely due to the cooling time of the PC layer being too slow. As shown in the thermal model (fig. 4.6(a)), an increase in barrier layer thickness results in a larger thermal capacitance. When the thermal capacitance is increased due to an increase in barrier layer thickness as well as a wider heater, the cooling rate of the switch may be too slow to amorphize the PC material. A switch with a 2 μm wide heater was pulsed using 2.94 W of power before failure, compared to the 1.68 W required to amorphize a similar switch with a 1 μm wide heater.

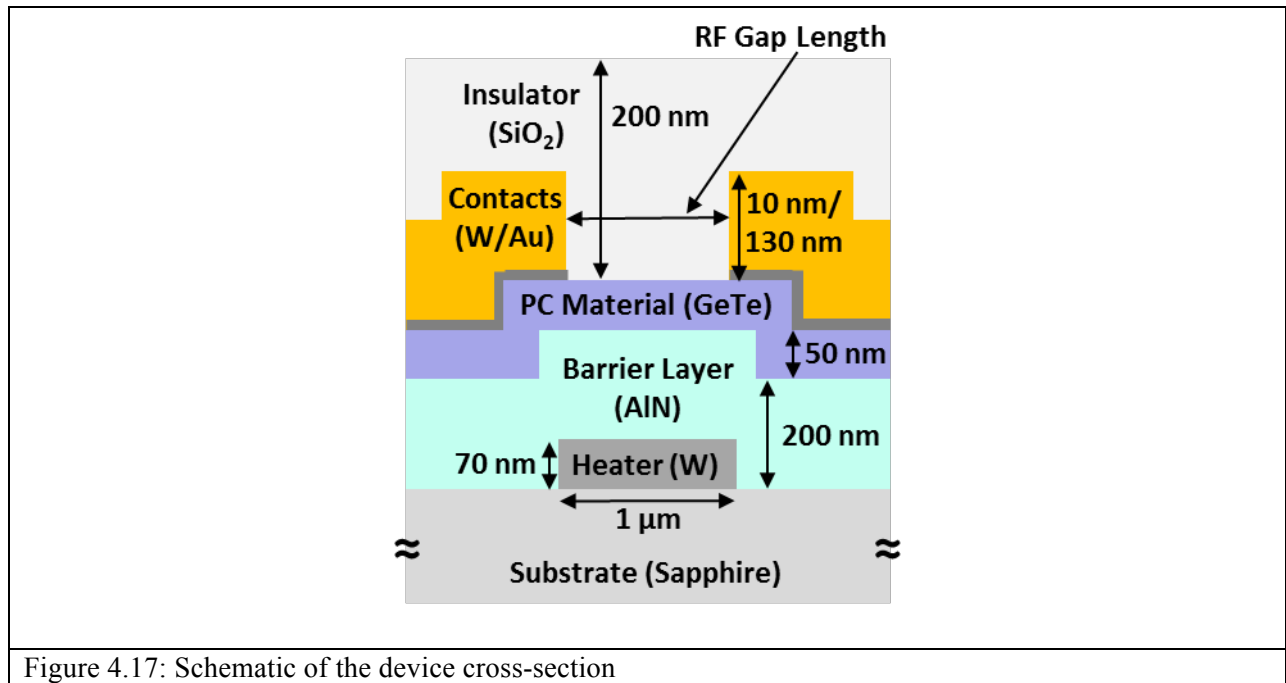


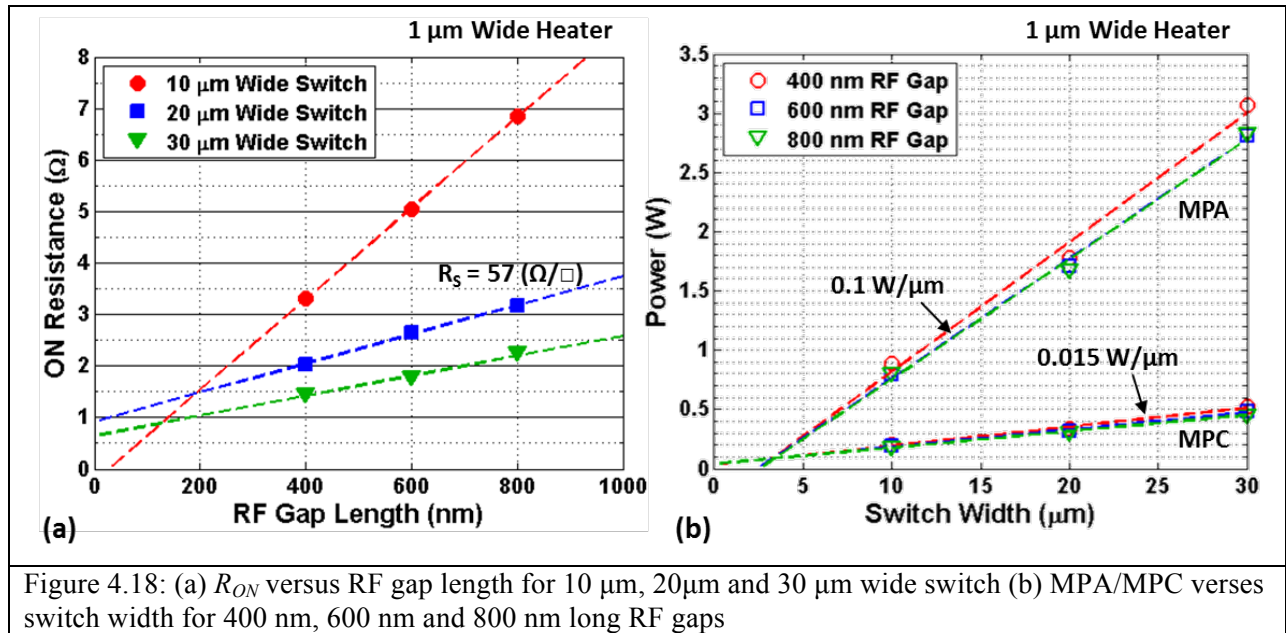
Figure 4.17: Schematic of the device cross-section

4.7.1 MPA and MPC

As seen previously for switches with a 1 μm wide heater, the sheet resistance of the film in the switch differs from that measured on the Van der Pauw and TLM structures. Fig. 4.18(a) shows R_{ON} versus RF gap length. The R_S extracted from the plot was 57 Ω/\square for the 20 μm and 30 μm wide switches while the 10 μm wide switch showed an R_S of 88 Ω/\square . The contact resistance for the 20 μm and 30 μm

wide switches was $19 \Omega\text{-}\mu\text{m}$ for two contacts. The measured R_s from the Van der Pauw structure was $72 \Omega/\square$ and $46 \Omega/\square$ off the TLM measurement. The reasons for these discrepancies are unknown.

The MPA and MPC were measured for switches with the $1 \mu\text{m}$ wide heater for all three RF gap lengths (fig 4.18(b)). The MPA increased by 0.1 W per micron of switch width and the MPC increased about 0.015 W per micron. Because of their high R_{ON} , the advantage of these switches cannot be determined until RF measurements are made. These switches required about 40% more power to turn off than the switches with 100 nm of GeTe and 100 nm of AlN.



4.8 Summary

This chapter discussed the DC measurement setup as well as the DC measurement results for four different sets of switches. It has been shown that doubling the thickness of the AlN barrier layer resulted in a modest increases in MPA (14%). The true benefits from thicker AlN will not be seen in the DC measurements but, rather, in the RF measurements that will be discussed in the next chapter.

Reducing the RF gap length reduces R_{ON} more than it increases the MPA. The minimum R_{ON} -MPA product of 2.4 Ω -W occurs at the shortest RF gap for the 50 nm thick GeTe. The cyclability of the switches still needs to be further explored as the R_{ON} increases after cycling the switch 50 times.

Increasing the width of the heater only increases the MPA of the switch. The switches currently have an R_{ON} that is dependent on the heater width. This effect is larger for longer RF gaps. This dependence must be explored further as narrower heaters are required to reduce the MPA of the switch. Increasing the width of the switch reduces the resistance of the switch at the expense of MPA. Increasing the thickness does not appear to increase the MPA and only reduces the R_{ON} . The lowest achieved R_{ON} -MPA product (1.3 Ω -W) was for a 20 μm wide switch with a 1 μm wide heater and a 400 nm RF gap with 100 nm of GeTe.

A reduction in the sheet resistance of the GeTe in the PC switch is required to make further gains in lowering R_{ON} . Despite great efforts taken to reduce the resistivity of the GeTe and to minimize the contact resistance from the contact metallization on standalone structures, the results have not successfully been transferred to the PC switch in this work. There is no apparent reason why such a transfer would not, ultimately, be possible.

Chapter 5: RF Switch Characterization

5.1 Abstract

This chapter discusses RF measurements made on 4-terminal RF PC switches using an AlN barrier layer to electrically isolate a high conductivity W heater. One-port and two-port S-parameter measurements were made on a variety of switch topologies. From these measurements, it has been determined that the lowest possible capacitance for a 20 μm wide is 10 fF. Increasing the AlN barrier past 170 nm does not reduce the OFF-state capacitance (C_{OFF}). Reducing the RF gap length from 900 nm to 400 nm increases the cutoff frequency (F_{CO}) from 4.5 THz to 7.2 THz despite an increase in C_{OFF} from 11.7 fF to 15.4 fF. These switches have also been seen to have excellent power handling capabilities up to 20 dBm in both the ON and OFF-states. The highest performing switch demonstrated has an ON-state resistance of 1.15 Ω and a C_{OFF} of 14.4 fF for an F_{CO} of 9.6 THz.

5.2 Introduction

The RF performance of the four terminal-inline PC switch is a critical factor in determining the switch's viability for use in reconfigurable RF circuits. RF switches require a low ON-state resistance ($< 1 \Omega$) while maintaining a high ON-OFF ratio (10^4) which is a specification that these PC switches are uniquely positioned to meet. They also require a low OFF-capacitance ($< 15 \text{ fF}$) to insure proper isolation of the RF-signal at higher frequencies ($> 10 \text{ GHz}$). As discussed earlier, a common figure of merit used for RF switches is cutoff frequency (F_{CO}), which is the frequency at which the magnitude of the off impedance is equal to the magnitude of the on impedance (as shown in *eq. 5.1*).

$$|R_{ON}| = \left| \frac{1}{j2\pi C_{OFF} f} \right| \quad (5.1)$$

Eq. 5.1 can be simplified further by solving for f as seen in *eq. 5.2*.

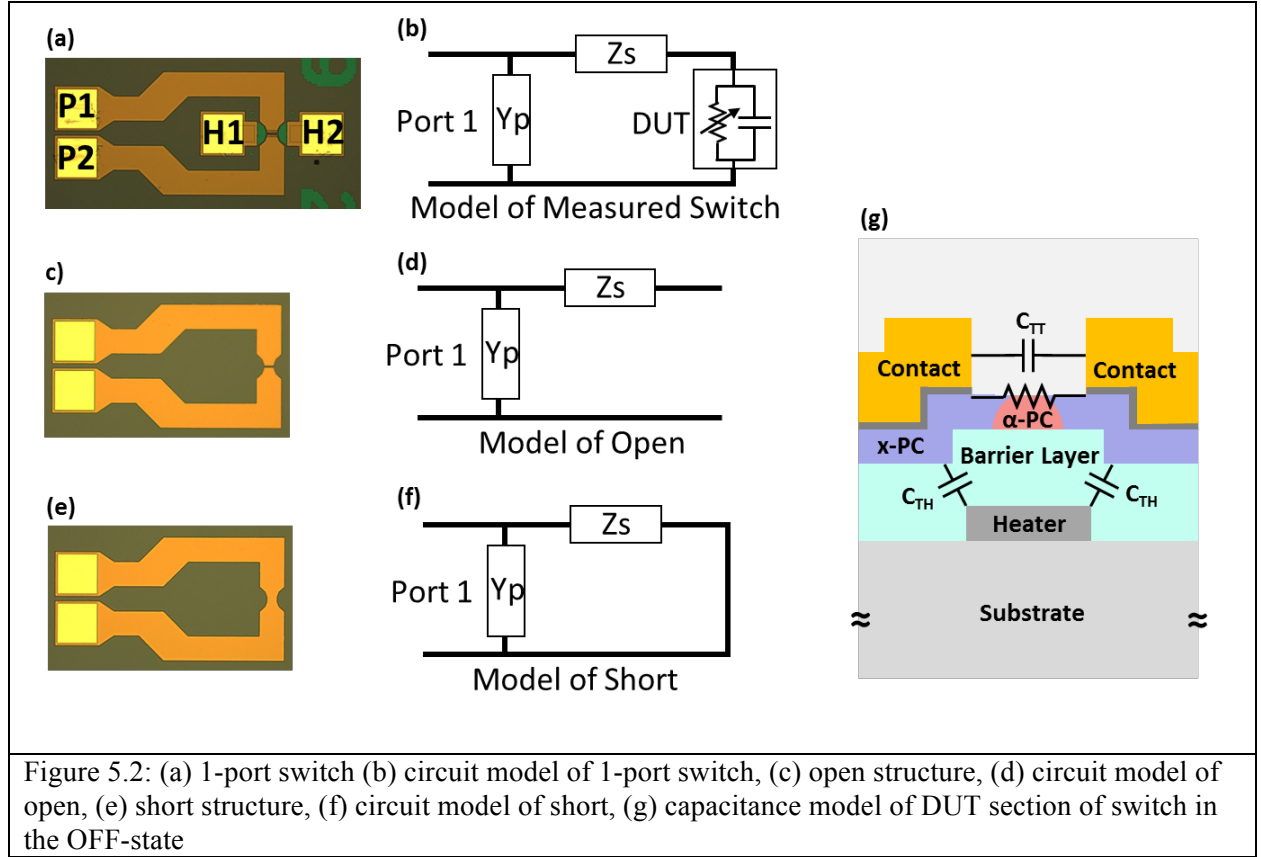
$$F_{CO} = \frac{1}{2\pi R_{ON} C_{OFF}} \quad (5.2)$$

RF switches with lower ON-state resistance and lower OFF-state capacitance result in a higher F_{CO} and are thus higher performing switches. This chapter will discuss the RF measurement test setup and de-embedding techniques used to extract the R_{ON} and C_{OFF} for the switches discussed in Chapter 4. All the measured switches will be compared to determine which parameters of the switch geometry result in the greatest increase in switch performance.

Two types of RF measurements were made for devices in this chapter: one-port S-parameter measurements and two-port S-parameter measurements. The first part of the chapter will discuss 1-port S-parameter measurements made on the devices that studied the effect of AlN thickness and RF gap length on RF performance. The second part of the chapter will use 2-port S-parameter measurements to study the effect of switch dimensions (switch width, heater width and RF-gap length) on RF performance. The effect of grounding the heater, cycling the switch and its power handling capabilities will also be examined.

5.3 One-Port S-Parameter Measurement Setup

One-port S-parameter measurements are made by applying an RF signal of varying frequencies but with constant power across the switch in both the ON and OFF-states. The amplitude and phase of the power reflected back from the switch can be used to determine the impedance of the switch, which can be interpreted through a model as its resistance and capacitance. One-port S-parameter measurements were conducted on the first two sets of devices discussed in Chapter 4.



The S-parameter measurements are made not just on the device (*DUT*) but on all the pads and traces that lead up to the device. The circuit model of the switch is shown in fig. 5.2(b), in which the *DUT* is modeled as a parallel combination of resistance (R_{DUT}) and capacitance (C_{DUT}). The pads and the traces leading up to the *DUT* can be modeled as a parallel admittance (Y_P) and a series impedance (Z_S), respectively (fig. 5.2(b)). To de-embed these parasitic elements (Y_P and Z_S), S-parameters of open (fig. 5.2(c) (d)) and short (fig. 5.2(e), (f)) structures are measured and converted to Y-parameters (Y_{OPEN} , Y_{SHORT}). Y_P (same as Y_{OPEN}) is then used to extract the series impedance, Z_S , using eq. 3.

$$Z_S = \frac{1}{Y_{SHORT} - Y_P} \quad (3)$$

The measured S-parameters of the switch (converted to Y-parameters, Y_{SWITCH}), Y_P and Z_S are then used to extract Z_{DUT} and Y_{DUT} using eq. 4.

$$Z_{DUT} = \frac{1}{Y_{DUT}} = \frac{1}{Y_{SWITCH} - Y_P} - Z_S \quad (4)$$

The resistance and capacitance of the DUT can then be calculated from Y_{DUT} using eq. 5 and eq. 6, respectively.

$$R_{DUT} = \frac{1}{\text{Re}(Y_{DUT})} \quad (5)$$

$$C_{DUT} = \frac{\text{Im}(Y_{DUT})}{2\pi f} \quad (6)$$

This de-embedding technique is necessary to extract an accurate R_{ON} and C_{OFF} of the device. Fig. 5.2(g) shows the capacitance model of the switch where C_{OFF} consists of a capacitor between the metal contacts (C_{TT}) in parallel with two capacitors in series that are between the heater and the PC layer (C_{TH}). There is also additional fringing capacitance that will be present between the heater pads and the switch. Because R_{ON} and C_{OFF} have some frequency dependence, the F_{CO} is calculated from the resistance and capacitance values at 5 GHz.

5.4 AlN Thickness Study, 105 nm vs. 170 nm

One-port S-parameter measurements were made on two switches discussed in Chapter 4, with a 550 nm RF gap and AlN barrier thicknesses of 105 nm and 170 nm. Fig. 5.3 shows their de-embedded R_{ON} and C_{OFF} as a function of frequency. The ON-state resistances of both switches are 2Ω for frequencies up to 15 GHz. The OFF-state capacitance of the switch, which has a significant contribution from the heater, C_{TH} (fig. 5.2(g)), is reduced from 15 fF to 10 fF when the AlN barrier thickness is increased from 105 nm to 170 nm. The F_{CO} increases from 5.2 THz for 105 nm of AlN to 7.7 THz for 170 nm of AlN. The F_{CO}/MPA ratio is 4.1 THz/W for 170 nm of AlN and 3.5 THz/W for 105 nm of AlN.

This shows that the F_{CO} increases by more than the MPA for the additional thickness of the AlN barrier layer and can therefore achieve a higher bandwidth for the same amount of power.

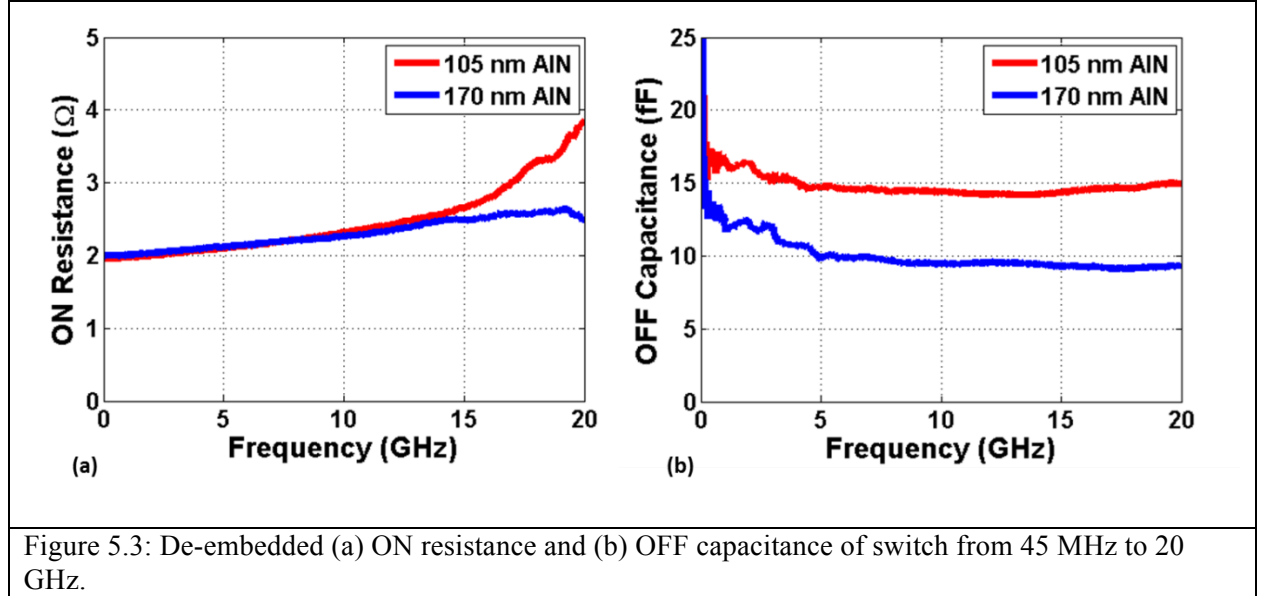
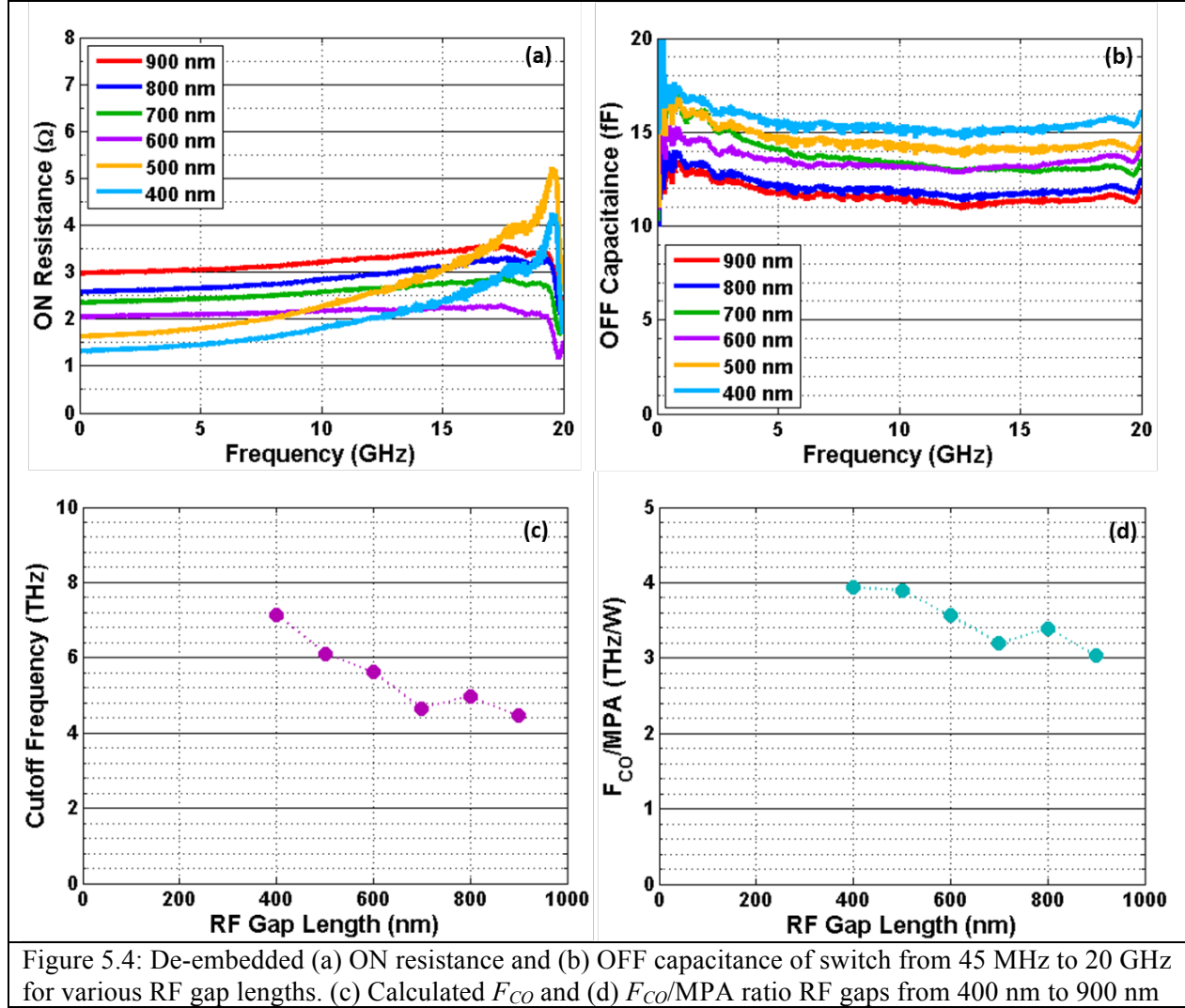


Figure 5.3: De-embedded (a) ON resistance and (b) OFF capacitance of switch from 45 MHz to 20 GHz.

5.5 The Effect of RF Gap

The effect of the RF gap length on R_{ON} and MPA has been shown in Chapter 4. Reducing the RF gap length reduces R_{ON} by more than the MPA increases; therefore, shorter RF gaps are favorable for their DC characteristics. However, as the RF gap is reduced, the capacitance between the contacts (C_{TT} in fig. 5.2(g)) increases. One-port S-parameter measurements were made on switches with RF gaps ranging from 400 nm long to 900 nm long. The de-embedded R_{ON} (fig. 5.4(a)) increases with RF gap length as seen from the DC measurements in Chapter 4. The de-embedded C_{OFF} (fig. 5.4(b)) decreases as expected with an increasing RF gap from 15.4 fF for a 400 nm gap down to 11.8 fF for a 900 nm gap. The F_{CO} (fig. 5.4(c)) increases with a decreasing RF gap length and is as high as 7.2 THz for a 400 nm RF gap. Therefore, R_{ON} decreases more than C_{OFF} increases. The F_{CO} /MPA ratio also increases with a decreasing

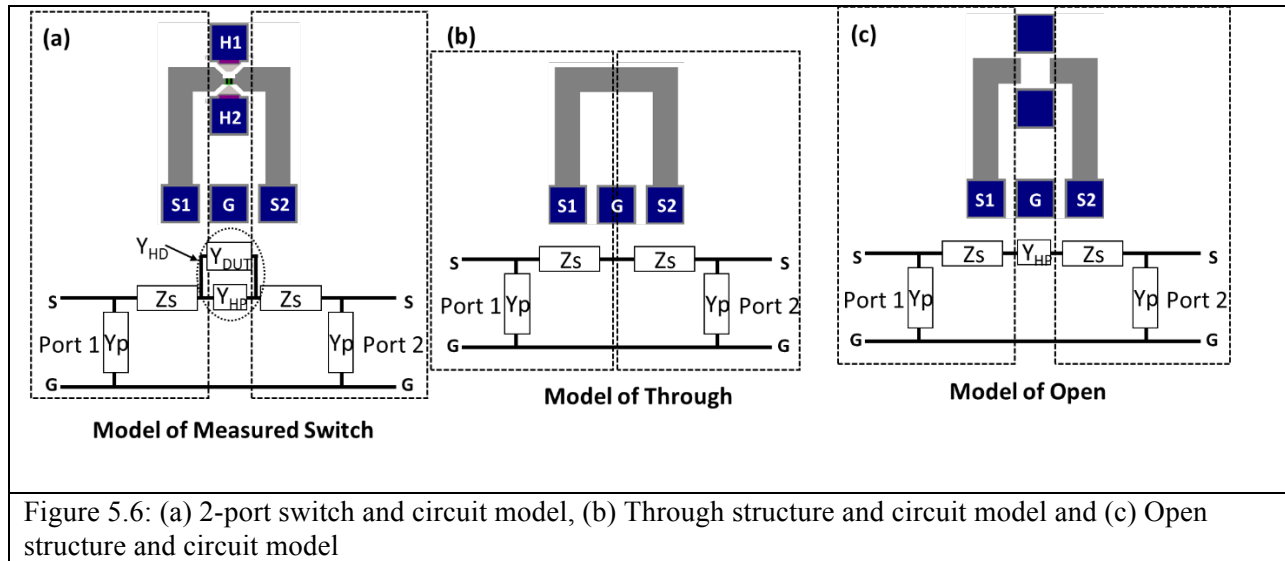
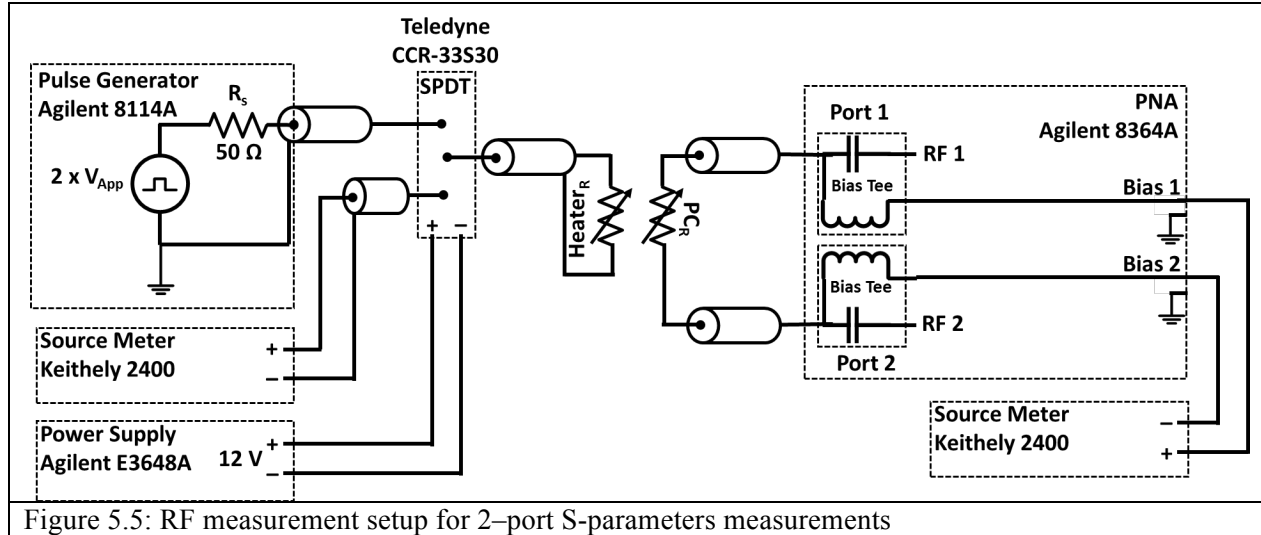
RF gap length (fig. 5.4(d)), showing that reducing the RF gap improves the RF performance of the switch without a significant penalty in power.



5.6 Two-Port S-Parameter Measurement Setup

The measurement setup for a 2-port S-parameter measurement is shown in fig. 5.5. Using a Signal-Ground-Signal (SGS) microwave probe on S1, G and S2 (fig. 5.6(a)), the device is placed in the signal path between port 1 and port 2 of the PNA. The DC resistance of the switch is measured using the bias tee for both ports in the PNA. The device is switched by pulsing the heater across H1 and H2

(fig. 5.6(a)) in the same way as the 1-port measurement setup. The 2-port S-parameter measurements were made from 45 MHz to 14 GHz with the heater probes up and landed on H1 and H2 (fig. 5.6(a)), with -15 dBm of RF power unless otherwise noted.



Just like with the 1-port measurements, the 2-port S-parameter measurements of the switch are made not only of the *DUT*, but also on the pads and traces leading up to the *DUT*. The circuit model of

the switch shows that the pads and traces from each port leading up to the *DUT* can be modeled as a parallel admittance (Y_P) and a series impedance (Z_S), respectively (fig. 5.2(a)). The *DUT* is in parallel with the admittance due to the heater pads (Y_{HP}) and is represented as Y_{HD} ($Y_{HD} = Y_{DUT} + Y_{HP}$). To de-embed these parasitic elements (Y_P , Z_S and Y_{HP}), 2-port S-parameters of through (fig. 6(b)) and open (fig. 5.6(c)) structures are measured. The S-parameters of the through structure are converted to Y-parameters (Y_{Thru}). Using the Y-parameter matrix of the through structure (as shown in eq. 7), Y_P and Z_S can be calculated using eq. 8 and eq. 9, respectively.

$$Y_{Thru} = \begin{pmatrix} Y_P + \frac{1}{2Z_S} & \frac{-1}{2Z_S} \\ \frac{-1}{2Z_S} & Y_P + \frac{1}{2Z_S} \end{pmatrix} \quad (7)$$

$$Y_P = Y_{Thru-11} + Y_{Thru-12} \quad (8)$$

$$Z_P = \frac{-1}{2Y_{Thru-12}} \quad (9)$$

A Y-parameter matrix can be made for the left (Y_L) and right side (Y_R) of the through using eq. 10 and eq. 11, respectively.

$$Y_L = \begin{pmatrix} Y_P + \frac{1}{Z_S} & \frac{-1}{Z_S} \\ \frac{-1}{Z_S} & \frac{1}{Z_S} \end{pmatrix} \quad (10)$$

$$Y_R = \begin{pmatrix} \frac{1}{Z_S} & \frac{-1}{Z_S} \\ \frac{-1}{Z_S} & Y_P + \frac{1}{Z_S} \end{pmatrix} \quad (11)$$

Converting Y_L and Y_R to T-parameters allows for the de-embedding of the pads and traces from the switch, as well as the open structure. The T-parameters of the switch and open structure are shown in *eq. 12* and *eq. 13*, respectively. T_{HP} are the T-parameters of the heater pads and T_{HD} are the T-parameters of the heater pads in parallel with the DUT.

$$T_{Switch} = T_L \cdot T_{HD} \cdot T_R \quad (12)$$

$$T_{Open} = T_L \cdot T_{HP} \cdot T_R \quad (13)$$

T_{HD} and T_{HP} can be calculated using *eq. 14* and *eq. 15*, respectively.

$$T_{HD} = T_L^{-1} \cdot T_{Switch} \cdot T_R^{-1} \quad (14)$$

$$T_{HP} = T_L^{-1} \cdot T_{Open} \cdot T_R^{-1} \quad (15)$$

The Y-parameters of the DUT are calculated by converting T_{HD} and T_{HP} to Y-parameters and using *eq. 16*.

$$Y_{DUT} = Y_{HD} - Y_{HP} \quad (16)$$

Y_{DUT} can then be converted back to S-parameters, while R_{DUT} and C_{DUT} of the device can be calculated from Y_{21} of the DUT (Y_{DUT-21}) using *eq. 17* and *eq. 18*, respectively.

$$R_{DUT} = \frac{1}{\text{Re}(-Y_{DUT-21})} \quad (17)$$

$$C_{DUT} = \frac{\text{Im}(-Y_{DUT-21})}{2\pi f} \quad (18)$$

This 2-port de-embedding technique is necessary to extract accurate S-parameters of the device, as well as R_{ON} and C_{OFF} .

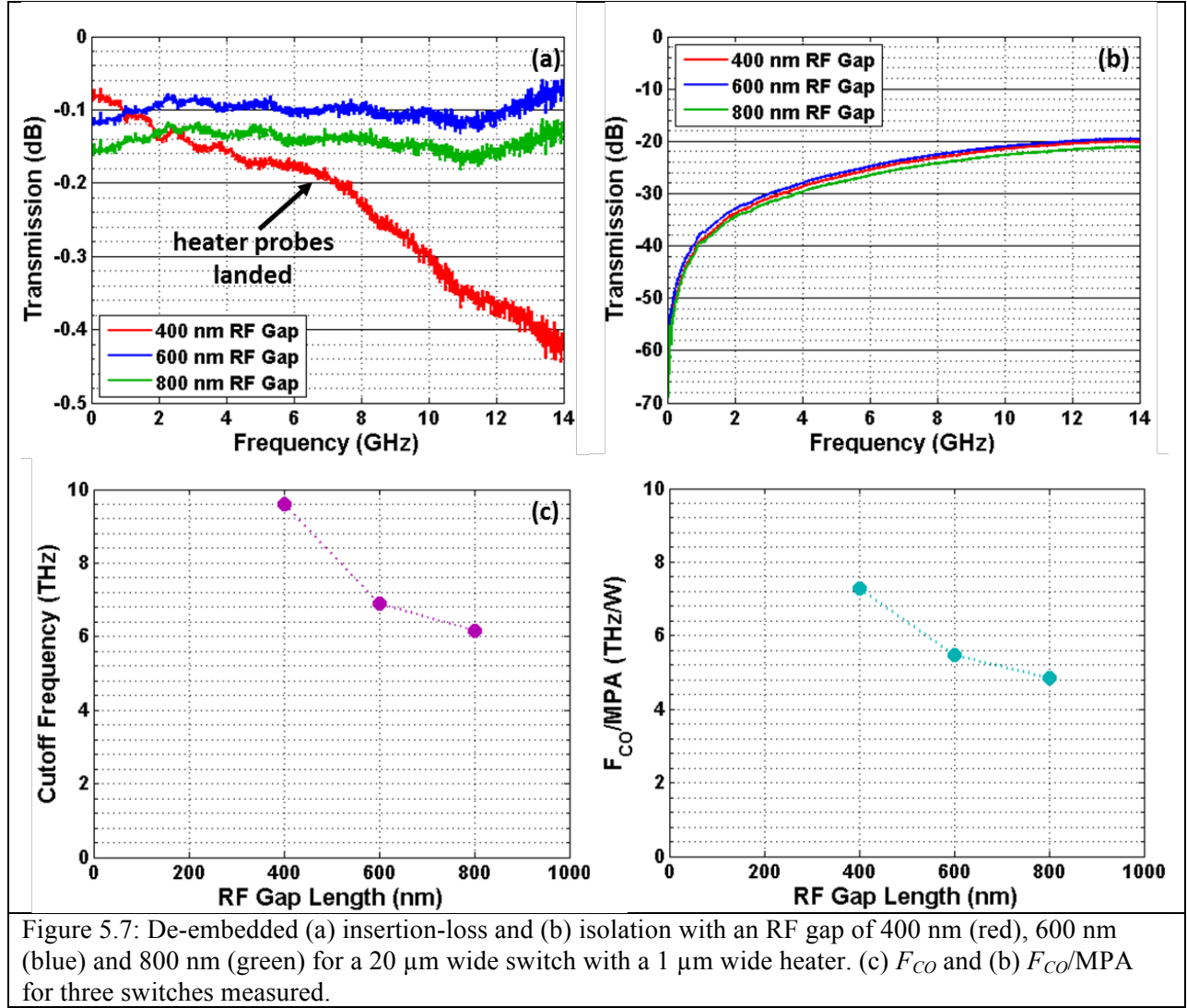
5.7 GeTe 100 nm Thick

5.7.1 RF Gap

Two-port measurements were made on two sets of switches. The first set of switches that will be discussed consisted of 100 nm GeTe with a 100 nm thick AlN barrier layer. The second set consisted of 50 nm of GeTe with a 200 nm thick AlN barrier layer, as previously discussed in Chapter 4. The S_{21} of three switches (20 μm wide with 1 μm wide heater) with RF gaps of 400 nm, 600 nm and 800 nm in the ON (fig. 5.7(a)) and OFF-state (fig. 5.7(b)) were measured from 45 MHz to 14 GHz with the heater probes in the up position. The insertion loss of the switches in the ON-state (fig. 5.7(a)) reduces with RF gap. This is consistent with the reduction in R_{ON} seen in the DC measurements. The insertion loss of the 400 nm RF gap becomes worse at higher frequencies. This is because the heater probes were accidentally still landed when this measurement was made. The effect of the heater being grounded will be discussed in the next section. The insertion loss of the 600 nm and 800 nm RF gap remains relatively constant up to 14 GHz with the 600 nm gap never dropping below -0.15 dB and the 800 nm gap never dropping below -0.175. The insertion loss of the 400 nm RF gap was about 0.05 dB higher than that of the 600 nm RF gap. Had the heaters probes been lifted during the measurement, it most likely would not have been below -0.1 dB. The isolation of the switches in the OFF-state is similar for all three RF gaps. The 800 nm RF gap has an isolation of 21 dB at 14 GHz, while the 400 nm and 600 nm have 20 db of isolation. The capacitance for the 400 nm RF gap is actually lower at 14.4 fF versus 15.4 fF for the 600 nm RF gap.

The F_{CO} of the switches is calculated from the R_{ON} and C_{OFF} at 4 GHz and plotted verses RF gap length (fig. 5.7(c)). The F_{CO} decreases with RF gap length just as it did in the previous set of samples discussed. The F_{CO} is as high as 9.6 THz for the switch with a 400 nm RF gap. The F_{CO} might have been even higher if the measurement was taken with the heater probes lifted, because the R_{ON} is a strong function of frequency when the heater probes are landed. The F_{CO}/MPA ratio also decreases with

increasing RF gap length. By increasing the GeTe thickness to 100 nm from 50 nm, the F_{CO}/MPA ratio increased from 4 THz/W to over 7 THz/W. Thus, reducing the RF gap length and increasing the GeTe thickness not only improves RF performance, but does so without significantly increasing power.



5.7.2 Grounding of Heaters

In El-Hinnawy et al., the authors discuss the effect of grounding the heaters on the RF performance of the switch [15]. When the switch is in the ON-state and the heaters are grounded, some

of the RF power that enters the switch leaks out to ground through the heater. C_{TH} (fig. 5.2(g)) acts as a shunt capacitor to ground and, as a result, increases the insertion loss of the switch at higher frequencies. When the switch is in the OFF-state, the shunt capacitance to ground actually increases the isolation of the switch resulting in a lower apparent C_{OFF} of the device. The grounded heater effect can also be seen when the heater probes are landed in this test setup. The insertion-loss and isolation of a 20 μm wide switch with a 1 μm wide heater and a 600 nm long RF gap can be seen in fig. 5.8. When the heater probes are landed, there is a significant increase in the insertion loss after 1 GHz. The S_{21} of the switch drops to -4.8 dB at 14 GHz and, when the heater probes are lifted, it never gets below -0.15 dB. The isolation of the switch increases by 2 dB when the heater probes are landed.

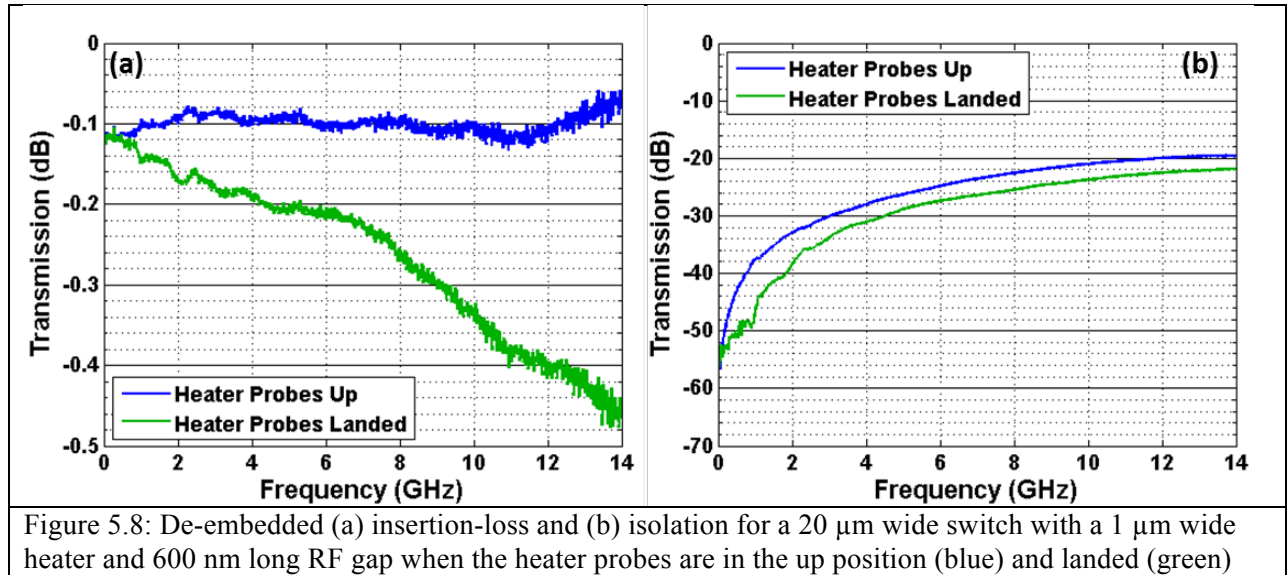


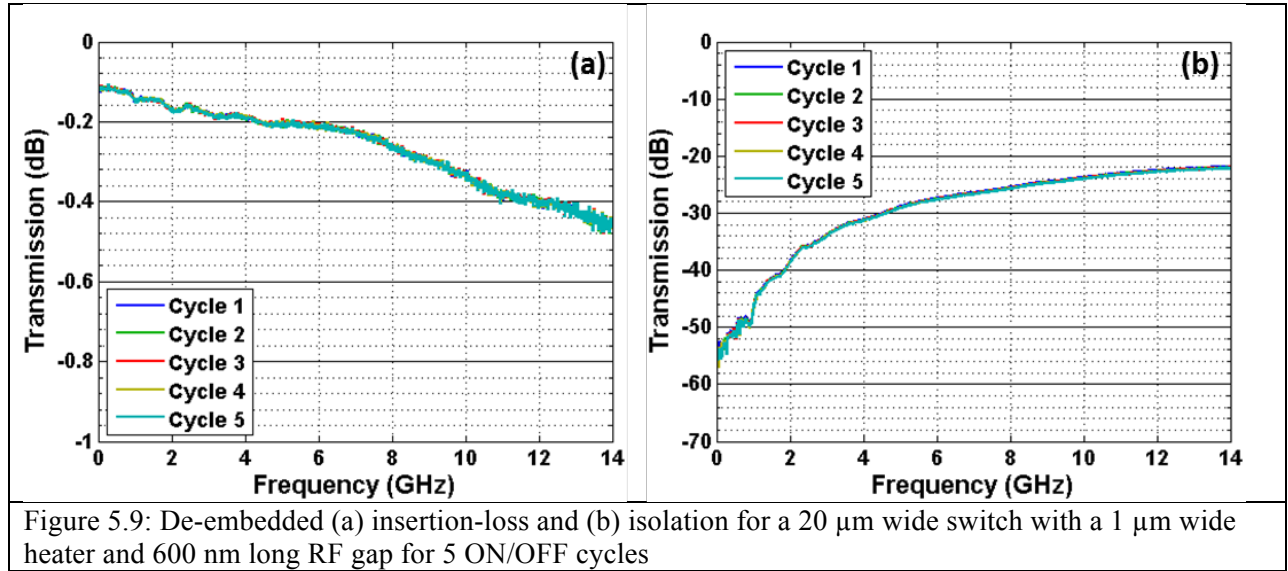
Table 5.1 summarizes the effect of landing the heater pads on R_{ON} , C_{OFF} and F_{CO} for 20 μm wide switches with a 1 μm wide heater. The switch resistance in the ON-state increases by about 0.1 Ω when the heater probes are landed. The increase in R_{ON} is even greater at higher frequencies. The capacitance in the OFF-state decreases over 4 fF when the heater probes are landed. This results in a significant increase in F_{CO} . The apparent F_{CO} of the switch increases from 10.5 THz to 13.7 THz when the heater probes are landed.

Switch Width (μm)	Heater Width (μm)	RF Gap Length (nm)	Probes Up R_{ON} (Ω)	Probes Landed R_{ON} (Ω)	Probes Up C_{OFF} (fF)	Probes Landed C_{OFF} (fF)	Probes Up F_{CO} (THz)	Probes Landed F_{CO} (THz)
20	1	400	1.05*	1.15	14.5	10.1	10.5	13.7
20	1	600	1.47	1.58	15.5	11.2	7.0	9.0
20	1	800	2.00	2.08	12.8	8.5	6.2	9

Table 5.1: Summary of RF switch performance with heater probes landed and in the up position
 * R_{ON} taken at 45 MHz and not 5 GHz because heater up data was not taken for this device

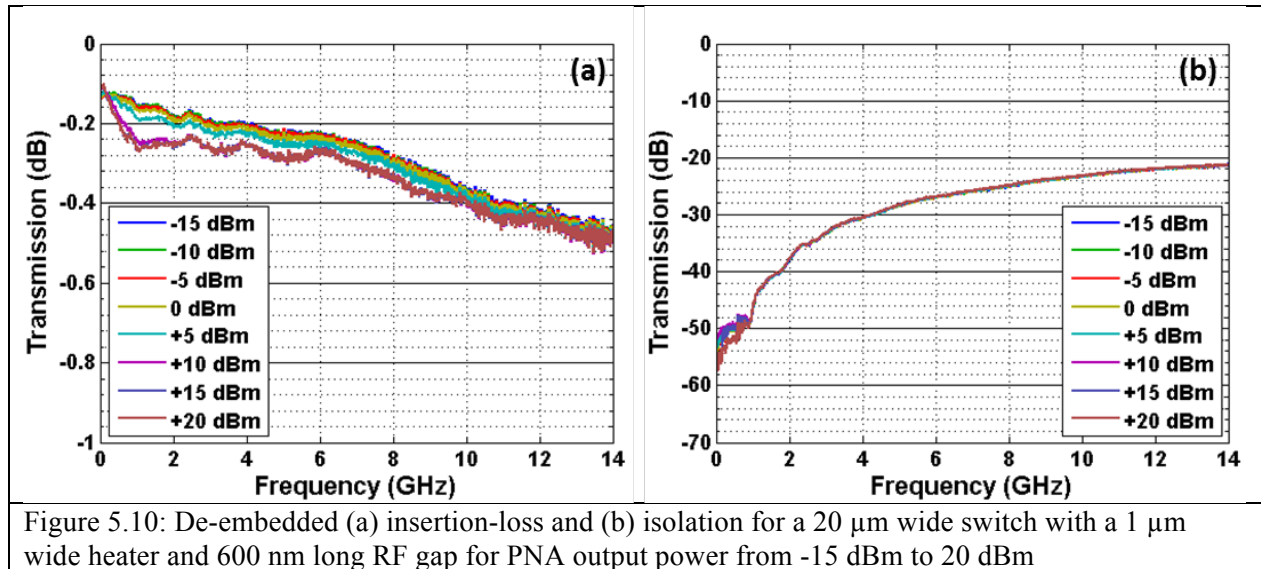
5.7.3 Cycling Data

Fig. 5.9 shows the insertion-loss and isolation of a 20 μm wide switch with a 1 μm wide heater and a 600 nm long RF gap for 5 ON-and-OFF cycles of the switch. The measurement was taken with the heater probes landed because the test was automated and the probe station does not have motorized control over the probes. Cycling the switch does not show any change in the RF performance of the switch.



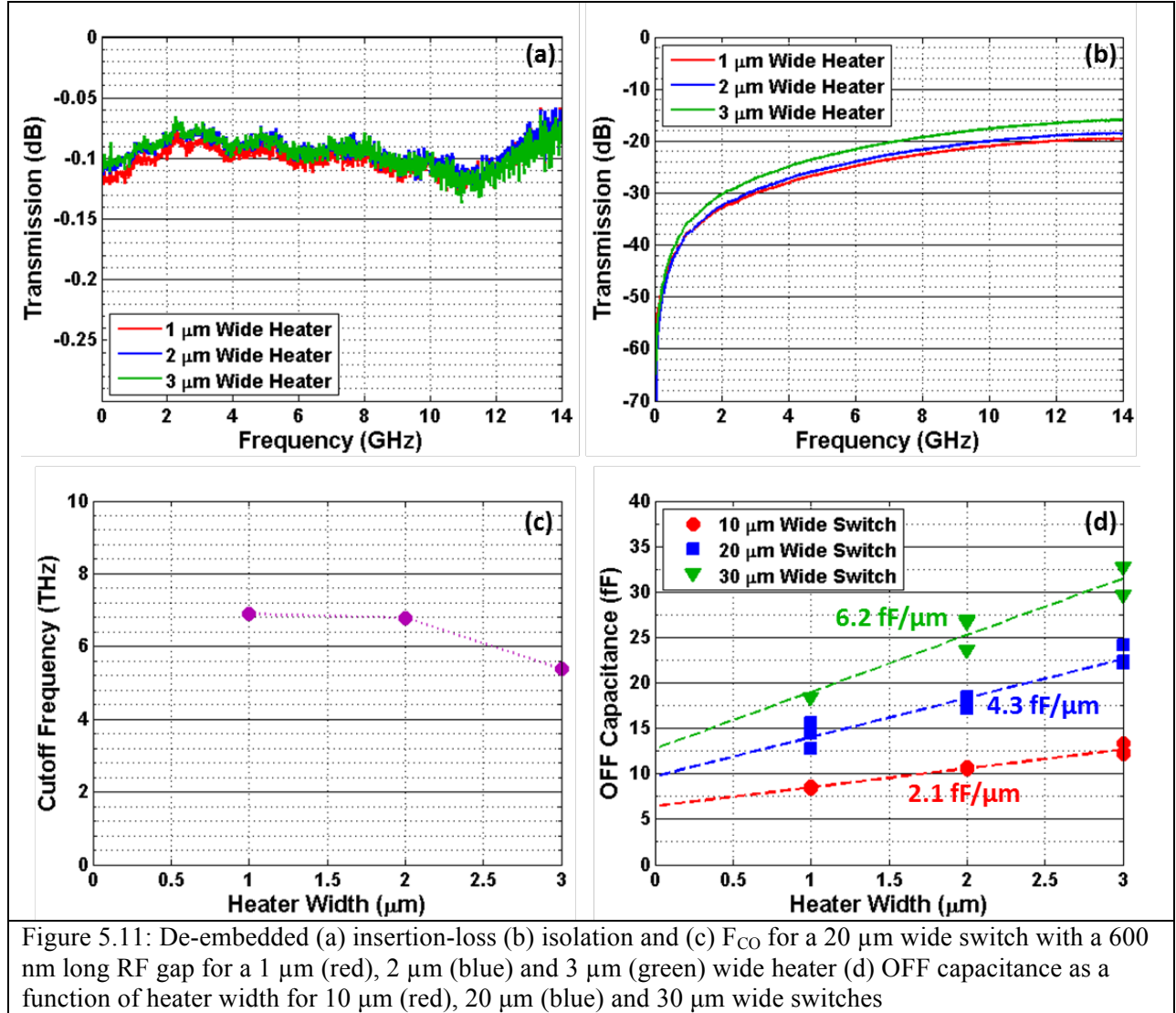
5.7.4 RF Switch Power Handling Capabilities

Another 20 μm wide switch with a 1 μm wide heater and a 600 nm long RF gap was tested to determine the effects of RF power on the RF performance of the switch. Normally, the S-parameter measurements are taken with an output power of -15 dBm from the PNA. The output power from the PNA was increased from -15 dBm to 20 dBm in 5 dBm increments and the S-parameters were measured for the switch in the ON-(fig. 5.10(a)) and OFF-state (fig. 5.10(b)). This test was also automated and therefore required the heater probes to be landed during the measurement. The output power did not affect insertion loss of the switch in the ON-state until it was above 5 dBm. At 10 dBm and above the insertion loss only increased by 0.1 dB at 1 GHz and reduced as the frequency increased. The output power did not affect the isolation of the switch in the OFF-state. The power handling capabilities of these types of switches are usually limited by their RF performance in the OFF state. In the OFF-state, the switches may be required to standoff large RF powers which in turn lead to large voltages. The large voltages across the switch could lead to the switch turning ON spontaneously due to ovonic memory switching [18]. This switch is able to standoff over 20 dBm of RF power (100 mW); however, this is only 3.2 V into a 50 Ω load. Higher RF power could not be tested because the PNA used had a maximum output power of 20 dBm. DC threshold voltage measurements have not been made on these devices.



5.7.5 Heater Width

The effect of the heater width on the insertion loss and isolation for a 20 μm wide switch with a 600 nm long RF gap is shown in fig. 5.11(a) and fig. 5.11(b), respectively. The insertion loss for the 1 μm heater is slightly higher than that for the 2 μm and 3 μm wide heaters for frequencies less than 10 GHz. The increase in insertion loss is due to a larger R_{ON} that is seen for the 1 μm wide heater. The isolation decreases for wider heaters. A 3 μm wide heater has 16 dB of isolation while a 1 μm wide heater has over 19 dB of isolation. This decrease in isolation is expected due to the larger OFF capacitance associated with a wider heater. The F_{CO} of the three switches decreases with heater width due to the increase in C_{OFF} . The difference in F_{CO} between a 1 μm and 2 μm heater is not as large due to a large R_{ON} for the 1 μm wide heater. Fig. 5.11(d) shows the OFF-state capacitance as a function of heater width for all three switch widths (10 μm , 20 μm and 30 μm). For a 20 μm wide switch, the capacitance increases by 4.3 fF per micron of heater width. For a heater width of “0” μm , the capacitance of the switch would still be 9.7 fF. That capacitance includes any fringing capacitance between the switch and the heater pads as well as C_{TT} (fig 5.2(g)). Increasing the width of the heater not only degraded the RF performance of the switch but also increased the power required to switch the device, thus making heater width a parameter that should be minimized.



5.7.6 Switch Width

The effect of the switch width on the insertion loss and isolation for switches with a 1 μm wide heater and 800 nm long RF gap are shown in fig. 5.12(a) and fig. 5.12(b), respectively. As expected, the insertion loss decreases with increasing switch width (fig. 5.12(a)). This is due to R_{ON} decreasing as switch width increases. For a 10 μm wide switch, the insertion loss is as high as 0.32 dB and reduces to 0.17 dB and 0.13 dB for a 20 μm switch and a 30 μm wide switch, respectively. The isolation of the switches in the OFF-state reduces as switch width increases (fig. 5.12(b)). This decrease in isolation is

due to an increase in C_{OFF} as switch width increases. The isolation for a 10 μm wide switch is 25 dB at 14 GHz; however, this reduces down to 21 dB and 18 dB for a 20 μm switch and a 30 μm wide switch, respectively. The F_{CO} increases for wider switches from 5.4 THz for a 10 μm wide switch to 6.4 THz for a 30 μm wide switch. This increase is because R_{ON} scales with switch width while C_{OFF} does not due the presence of fringing capacitance between the switch and the heater pads. The fringing capacitance can be determined by plotting C_{OFF} as a function of switch width (fig. 5.12(d)) for each width of heater (1 μm , 2 μm and 3 μm). The capacitance for a “0” μm wide switch is 3.7 fF for all heater widths. This capacitance is the fringing capacitance of the switch. For a switch with a 1 μm wide heater, the OFF-state capacitance increases by 0.51 fF/ μm of switch width when the AlN barrier layer is 100 nm thick. Using the capacitance for a “0” μm wide heater (fig. 5.11(d)) along with the capacitance from a “0” μm wide switch, C_{TT} can be calculated to be 0.3 fF/ μm of switch width. This shows that the contact metallization contributes more capacitance to the switch than does the heater.

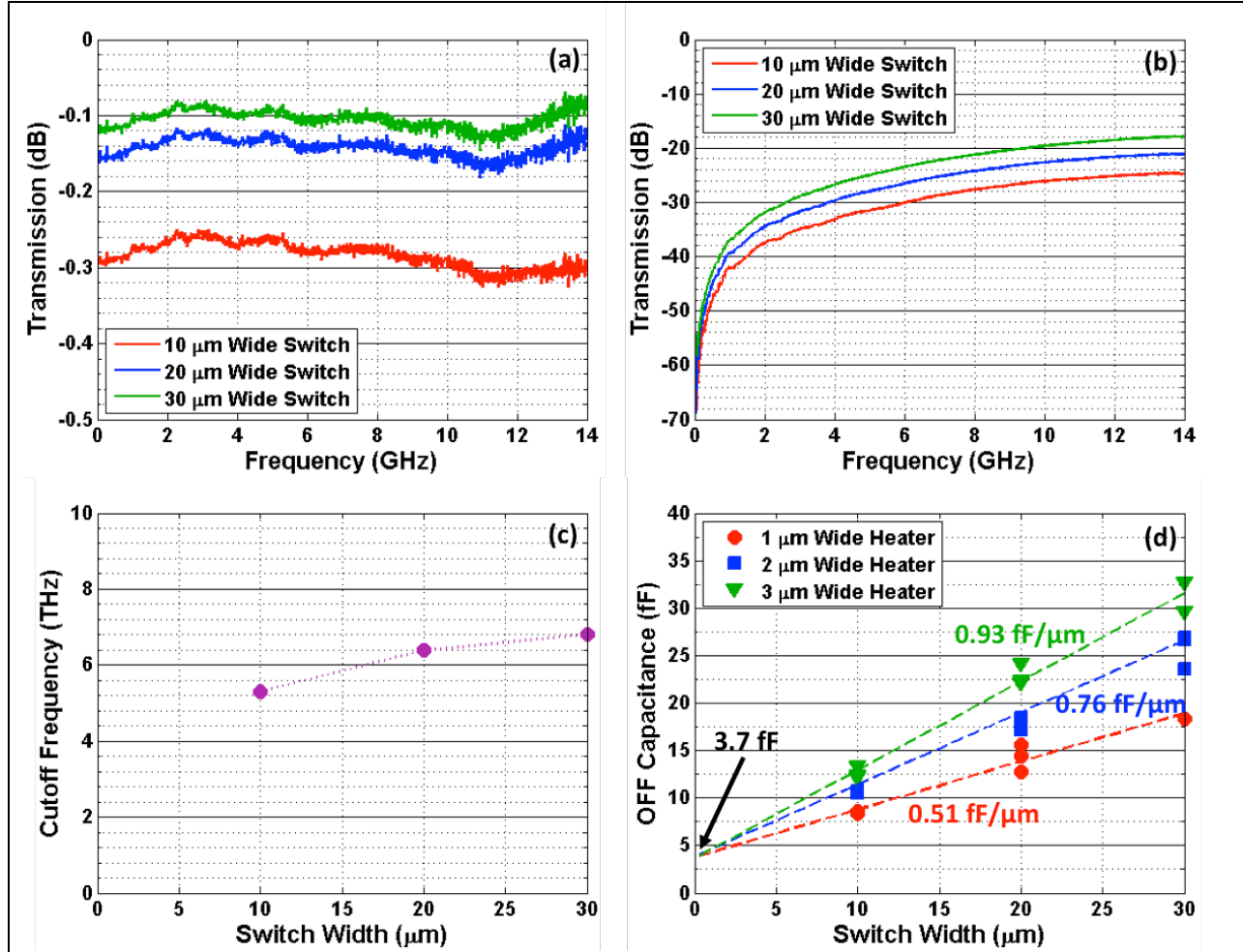
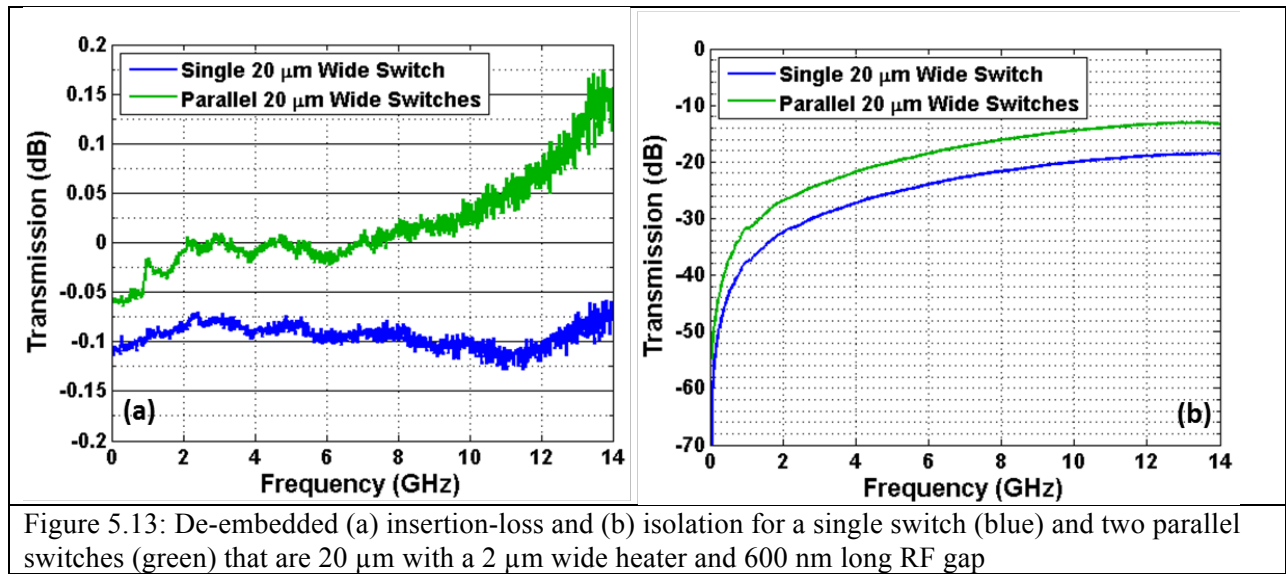


Figure 5.12: De-embedded (a) insertion-loss (b) isolation and (c) F_{CO} for a 10 μm (red), 20 μm (blue) and 30 μm (green) wide switches with a 600 nm long RF gap for a 1 μm wide heater (d) OFF capacitance as a function of switch width for 1 μm (red), 2 μm (blue) and 3 μm wide heaters

5.7.7 Parallel Switches

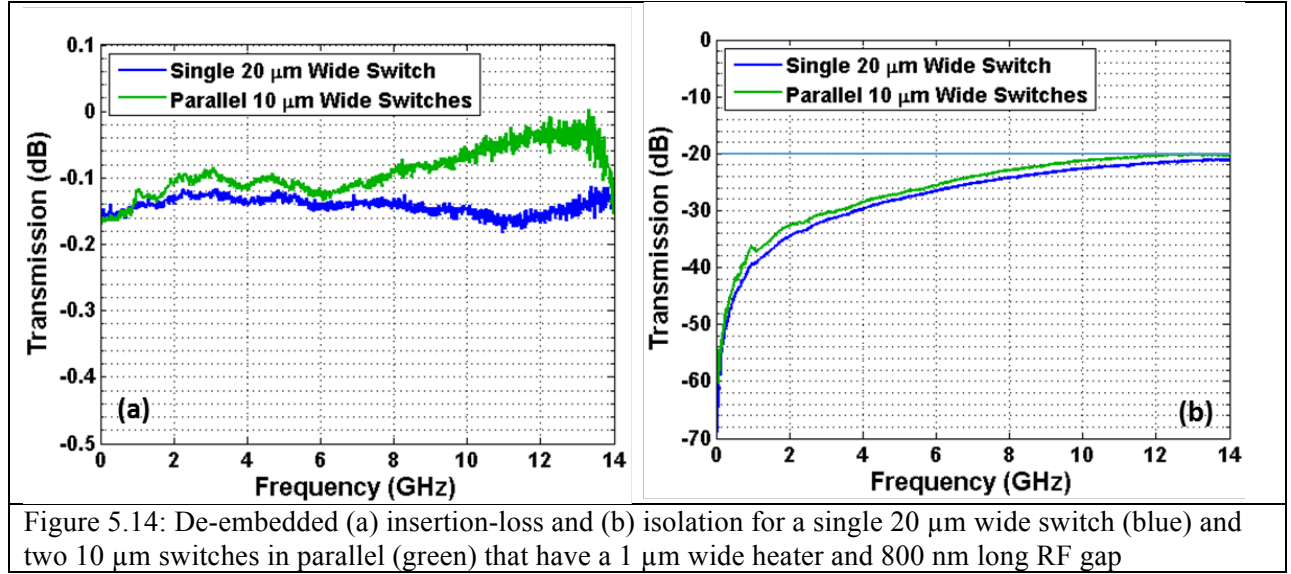
The use of two parallel switches of equivalent size has been shown in Chapter 4 to reduce the DC resistance of the switch by almost in half. The effect of two switches in parallel on RF performance still needs to be further explored. The insertion loss and isolation of a 20 μm wide switch with a 2 μm wide heater and 600 nm long RF gap are shown as a single switch (blue) and as two switches in parallel (green) in fig. 5.13(a) and fig. 5.13(b), respectively. The use of another switch in parallel significantly reduces the insertion loss from 0.1 dB to 0.05 dB at low frequencies (<1 GHz). At frequencies above 7 GHz,

there appears to be a gain in the parallel switches. This gain is most likely due to a resonance from the traces that were not completely de-embedded out of the measurement. As expected, the isolation of the two switches in parallel is significantly lower due to an increase in C_{OFF} (17.1 fF to 32.2 fF). The isolation drops from 18 dB for 1 switch to 13 dB for two switches in parallel. The F_{CO} for the parallel switch is lower (5.8 THz) than the single switch (6.8 THz) because R_{ON} has a large frequency dependence (0.6Ω at 45 MHz and 0.85Ω at 4 GHz) that is not present in the single switch. This is more evidence that the parallel switches are not fully de-embedded.



The previous example of parallel switches would be used in applications where a low R_{ON} and minimal insertion loss are required at the expense of C_{OFF} and isolation. However, parallel switches can also be used to reduce the voltage required to turn off a switch as shown in Chapter 4. Fig. 5.14 shows the insertion loss and isolation for a single 20 μm wide switch (blue) and two 10 μm wide switches in parallel (green). The switches measured have a 1 μm wide heater and an 800 nm long RF gap. The insertion loss for both switches at low frequencies (< 2 GHz) is 0.16 db. As the frequency increases, the insertion loss for the parallel switches reduces further as was seen in the previous example of parallel switches. The isolation for the parallel switches is slightly worse (20 dB for the parallel switches and

21 dB for the single switch) because of a slightly higher C_{OFF} (14.4 fF for the parallel switches and 12.8 fF for the single switch). The additional capacitance is due to the additional fringing associated with the extra heater pad. As a result, the F_{CO} reduced from 6.2 THz to 5.3 THz by using two 10 μm wide switches in parallel instead of a single 20 μm wide switch.

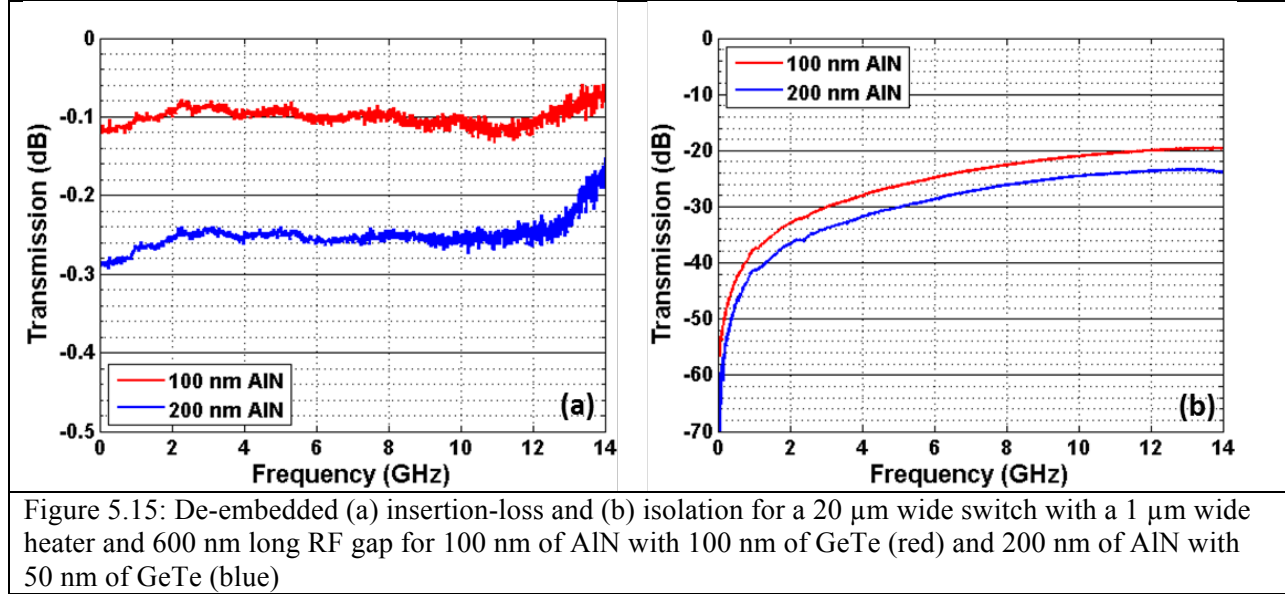


5.8 AlN 200 nm Thick

5.8.1 AlN 100 nm vs. 200 nm

The last devices that will be discussed in this chapter have 50 nm of GeTe with a 200 nm thick AlN barrier layer. As discussed in the previous chapter, these devices were fabricated to determine how thick the AlN barrier could be while still maintaining switch functionality and whether the capacitance of the switch could be reduced below the 10 fF measured for 170 nm of AlN. Fig. 5.15 compares the isolation and insertion loss of two switches (20 μm wide, 1 μm wide heater and 600 nm RF Gap): one with 100 nm of GeTe and 100 nm of AlN (red) and the other with 50 nm of GeTe and 200 nm of AlN (blue). As expected, the insertion loss (fig. 5.15(a)) is much higher for the switch with 200 nm of AlN because the GeTe is half as thick (R_{ON} is 3.35 Ω for 50 nm GeTe and 1.48 Ω for 100 nm GeTe).

However, the additional AlN does significantly increase the isolation of the switch in the OFF-state from 20 dB for 100 nm of AlN to 24 dB for 200 nm of AlN at 14 GHz. This increase in isolation is due to a reduction in C_{OFF} from 15.6 fF to 10.1 fF.



5.8.2 OFF-Capacitance

The OFF-capacitance of the switches as a function of switch width can be seen in fig. 5.16. The capacitance increases for switches with shorter RF gaps. The fringing capacitance of the switches that can be extracted from the y-intercept of the fit are between 3.3 fF and 4.4 fF, which is similar to the 3.7 fF that was seen for the previous set of switches. The slope of the fit is as low as 0.26 fF/ μm for an 800 nm RF gap and increases to 0.4 fF/ μm for a 400 nm RF gap. The three RF gaps have an average slope of 0.32 fF per micron of switch width with 3.9 fF of fringing capacitance. For 100 nm AlN, the slope of the fit for a 1 μm wide heater was 0.51 fF/ μm . It was previously noted that the capacitance associated with C_{TT} was 0.3 fF/ μm of the 100 nm thick AlN, which should not be dependent on AlN thickness. Therefore when 200 nm of AlN is used, the capacitance attributed by the heater is 0 fF. For the first set of samples discussed in this chapter, C_{OFF} for 170 nm of AlN was 10 fF. For a similar device with 200 nm AlN, the

capacitance is 10.1 fF. This suggests that the capacitance of a 20 μm wide switch can never be below 10 fF and that going above 170 nm of AlN has no benefit to capacitance. Additionally, it requires power to turn the switch off. The 10 fF limit is also seen in fig. 5.11(d) where the capacitance of a 20 μm switch with a “0” μm wide heater is 9.7 fF.

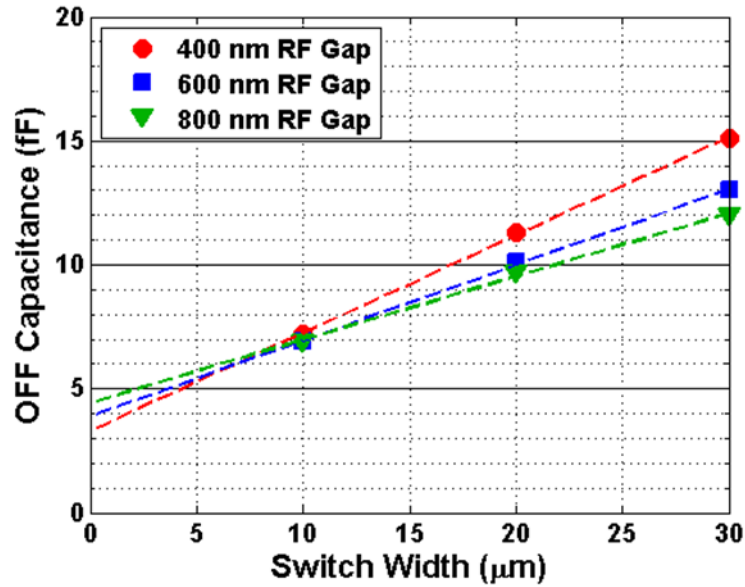
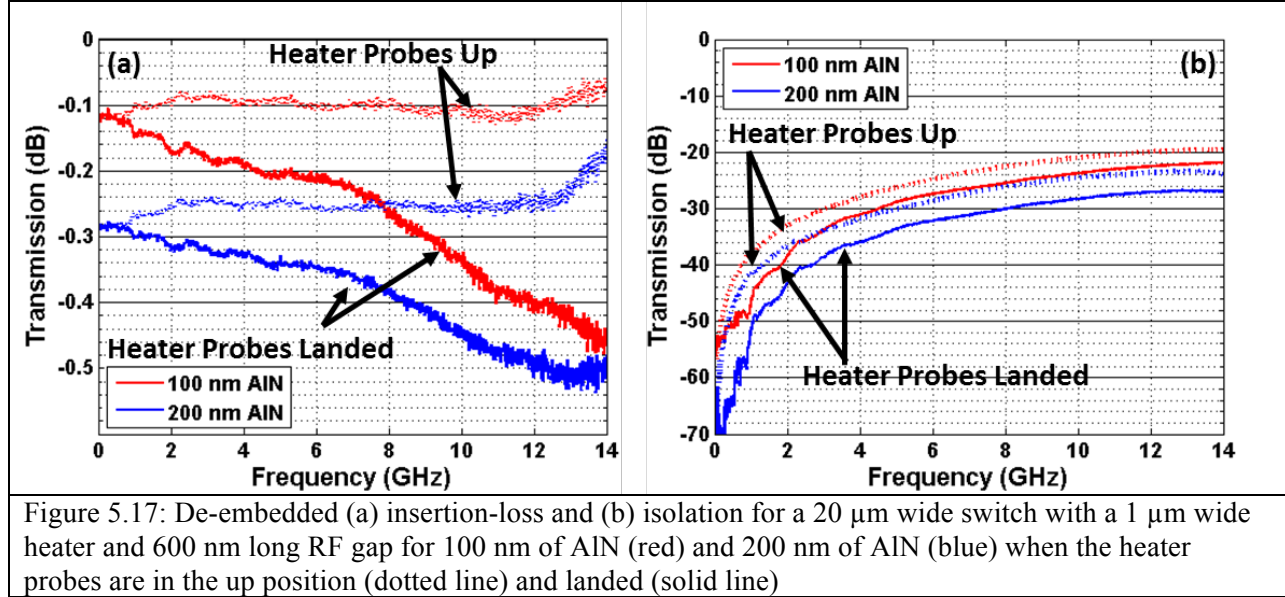


Figure 5.16: OFF-capacitance as a function of switch width for an RF gap of 400 nm (red), 600 nm (blue) and 800 nm (green)

5.8.3 Grounded Heaters

The effect on the insertion loss and isolation of having the heaters probes landed for a switch with 100 nm AlN (red) and 200 nm of AlN (blue) is shown in fig. 5.17. The difference in insertion loss at low frequencies ($< 1\text{GHz}$) is due to the larger R_{ON} for the switch for the 200 nm of AlN that was discussed earlier. However, the increase in the insertion loss is less severe for the thicker AlN. When the heater probes are up, the difference in insertion loss at 10 GHz is about 0.15 dB. However, when they are landed, the difference is only 0.1 dB. This reduction is due to a smaller shunt capacitance to ground from the increase in AlN thickness. The additional AlN also positively affects the isolation of the switch when the heater probes are landed. The isolation for 100 nm of AlN increases by about 2 dB when the heater

probes are landed and by 3 dB for 200 nm of AlN. This shows that increasing the AlN thickness has benefits if the switch design requires the heater to be grounded during operation.



5.9 Switch Dimension Comparison

In Chapter 4, the $MPA \cdot R_{ON}$ product of a switch was introduced to compare the different switches fabricated. The goal of that figure of merit was to show how much power was needed for a 1Ω switch with different switch dimensions. A lower $MPA \cdot R_{ON}$ product signified a better, more efficient switch. In this chapter, the F_{CO} of a switch was calculated to determine the RF performance of the switch and the F_{CO}/MPA ratio was used to demonstrate how much RF performance a given switch topology has for 1 W of power. However, the F_{CO}/MPA ratio can only be used to compare switches of the same width because, as switch width increases, the MPA increases by more quickly than does the F_{CO} . A new metric must be used to compare switches of different widths. The metric that will be used is the $F_{CO}/MPA \cdot R_{ON}$ ratio. Switches with a higher $F_{CO}/MPA \cdot R_{ON}$ are more desirable because they have higher RF performance, which results in a more efficient switch. This new metric will be used to compare all switch dimensions (switch width, heater width, RF gap length, AlN thickness and GeTe thickness) to determine which dimensions are the most important in maximizing the performance of the switch.

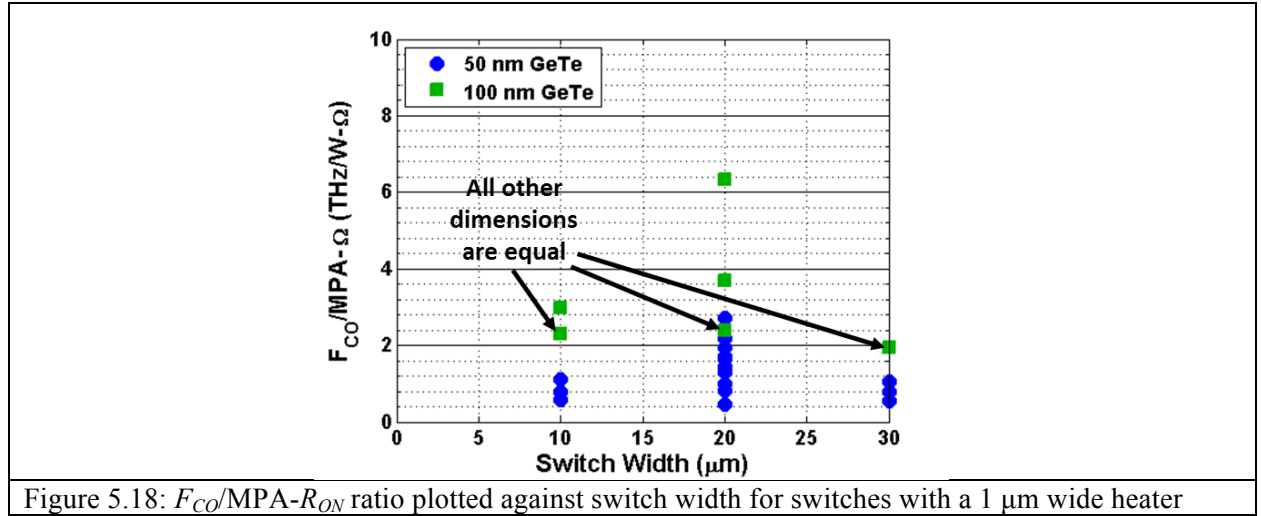
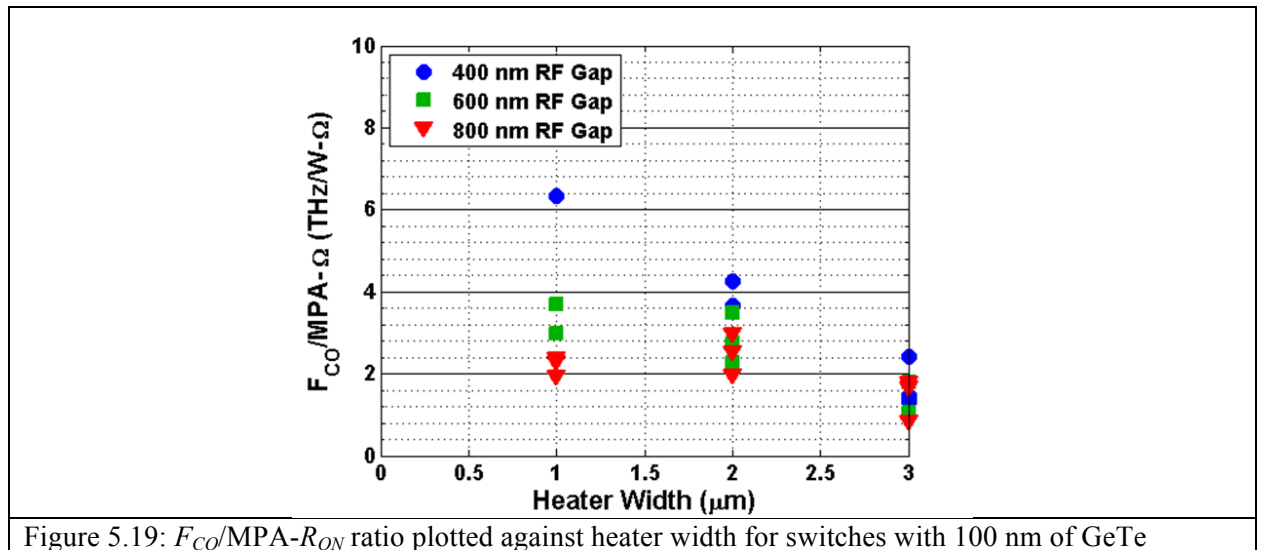


Fig. 5.18 shows the $F_{CO}/MPA-R_{ON}$ ratio plotted against switch width. For a better comparison only switches with a 1 μm heater were included in the plot. The plot suggests that 20 μm wide switches have significantly better performance. However, the majority of the switches fabricated were 20 μm wide which skews the plot. The switches that are marked with an arrow in fig. 5.18 have the same switch dimensions. The plot shows that 20 μm wide switches are slightly better, but it is not as significant as the plot suggests. This is expected because, while the F_{CO} does scale slightly with heater width, the $MPA-R_{ON}$ product should not.



The $F_{CO}/MPA-R_{ON}$ ratio is plotted against heater width for switches with 100 nm of GeTe in fig. 5.19. Switches with different RF gaps are color-coded. Reducing the heater width not only reduces the MPA of the switch but also the OFF-state capacitance, making narrow heaters ideal. The $F_{CO}/MPA-R_{ON}$ ratio is not as high for the 600 nm and 800 nm RF gap switches with a 1 μ m wide heater because of their dependence of R_{ON} on heater width.

Increasing the GeTe thickness significantly improves the performance of the switch. Fig. 5.20 shows the $F_{CO}/MPA-R_{ON}$ ratio plotted against GeTe thickness for 20 μ m wide switches with 1 μ m wide heaters and 100 nm of AlN. For each increase in RF gap, the $F_{CO}/MPA-R_{ON}$ ratio nearly doubles. The highest $F_{CO}/MPA-R_{ON}$ ratio is 6.3 THz/W- Ω in a switch with 100 nm of GeTe and only 2.7 THz/W- Ω with 50 nm of GeTe. Increasing the GeTe thickness results in R_{ON} decreasing without the MPA increasing.

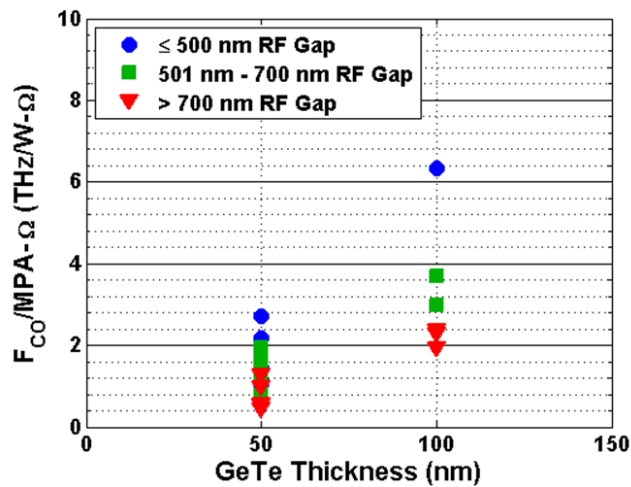
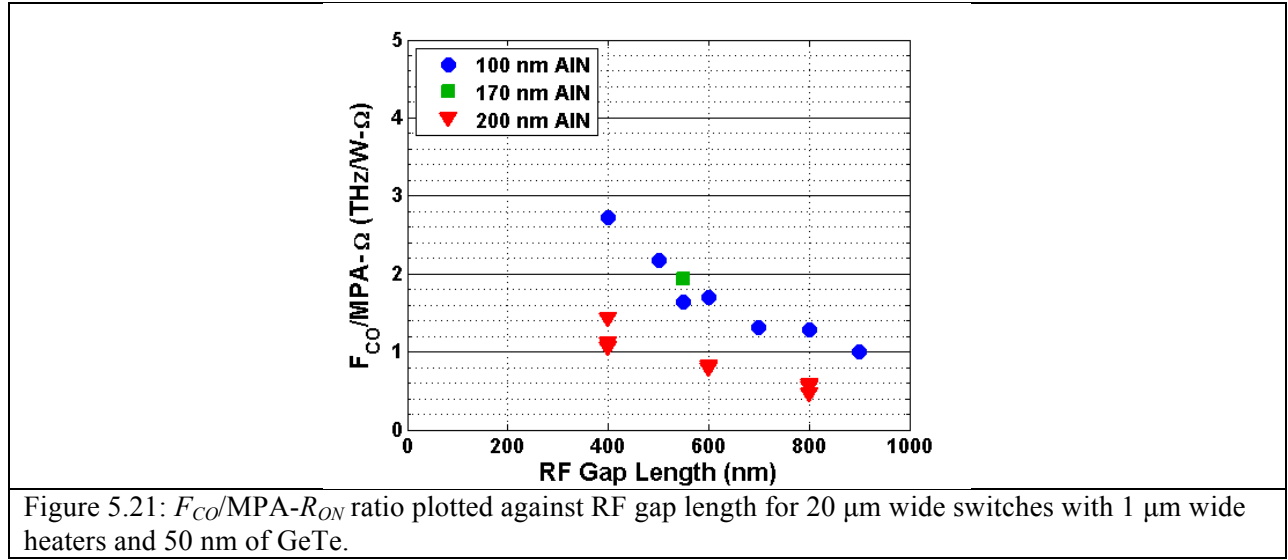


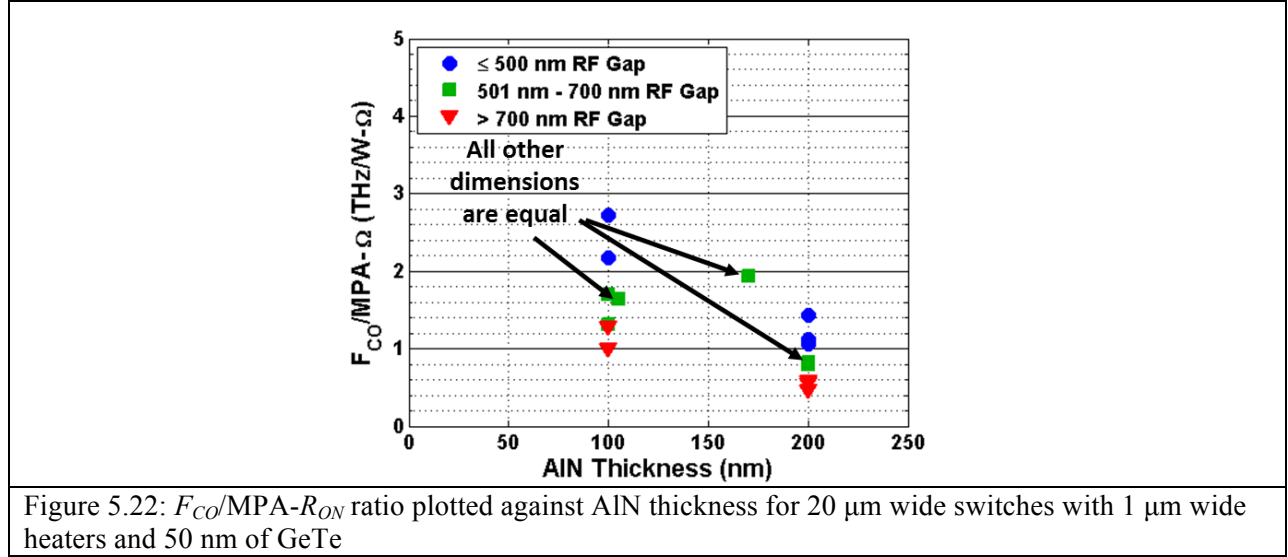
Figure 5.20: $F_{CO}/MPA-R_{ON}$ ratio plotted against GeTe thickness for 20 μ m wide switches with 1 μ m wide heaters and 100 nm of AlN

The $MPA \cdot R_{ON}$ product as well as the F_{CO} both improve as the RF gap shrinks. Therefore, it not surprising that the $F_{CO}/MPA \cdot R_{ON}$ ratio also increases as the RF gap becomes narrower. The $F_{CO}/MPA \cdot R_{ON}$ ratio is plotted against RF gap length for 20 μm wide switches with 1 μm wide heaters and 50 nm of GeTe in fig. 5.21. For each AlN thickness, the $F_{CO}/MPA \cdot R_{ON}$ ratio increases as the RF gap becomes narrower. The $F_{CO}/MPA \cdot R_{ON}$ ratio nearly triples by reducing the RF gap from 900 nm to 400 nm long. Reducing the RF gap length is an effective way to increases the performance of the switch.



In the beginning of the chapter, it has been shown that increasing the AlN thickness from 105 nm to 170 nm improves the F_{CO}/MPA ratio for the same R_{ON} . The RF measurements on the 200 nm thick AlN switches reveal that the OFF- state capacitance of the switch does not reduce below 10 fF. Therefore, it should not be expected that continuing to increase the AlN thickness would result in higher performing switches. Fig. 5.22 shows the $F_{CO}/MPA \cdot R_{ON}$ ratio plotted against AlN thickness for 20 μm wide switches with 1 μm wide heaters and 50 nm of GeTe. The plot shows that increasing the AlN thickness to 200 nm actually reduces the $F_{CO}/MPA \cdot R_{ON}$ ratio. As shown in Chapter 4, part of the reduction is due to the higher than expected R_{ON} for the switches with 200 nm of AlN. Three switches are marked in fig. 5.22 that have similar RF gaps. This demonstrates that there is some benefit in increasing

the AlN thickness to 170 nm but it is very minimal. Increasing the AlN thickness above 170 nm does not have any benefits because C_{OFF} does not continue to reduce.



From the $F_{CO}/MPA-R_{ON}$ ratio plots above, it becomes obvious that the three major parameters of the switch that must be focused on are heater width, GeTe thickness and RF gap length. The switch width and AlN thickness are not major factors in the performance of the switch. Using 100 nm of GeTe with a 1 μm wide heater and a 400 nm RF gap allows for a $F_{CO}/MPA-R_{ON}$ ratio in excess of 6 THz/W-Ω.

5.10 Summary

This chapter discussed the RF performance of four sets of switches fabricated using both 1-port and 2-port measurement techniques. Increasing the AlN thickness from 105 nm to 170 nm does reduce C_{OFF} without significantly increasing the MPA of the switch. However, it has been shown that increasing the AlN thickness beyond 170 nm does not further reduce C_{OFF} and that the minimum capacitance for a 20 μm wide switch with a 1 μm wide heater is approximately 10 fF. Therefore, there is no advantage in having the AlN barrier layer above 170 nm thick.

Reducing the RF gap length has been shown to significantly improve RF performance for multiple sets of switches. The resistance of the switch in the ON-state reduces by more than the OFF-state capacitance and MPA increase. Increasing the GeTe thickness also improves the RF performance of the switch without increasing the MPA.

Measuring the 2-port S-parameters with the heater probes landed significantly alters the RF performance of the switch. When the heater probes are landed, an additional shunt capacitance to ground is present causing the insertion loss to increase at higher frequencies when the switch is ON. However, the isolation of the switch in the OFF-state improves when the heater probes are down and reduces the effective OFF-capacitance of the switch.

The RF performance of the switch does not seem to change with cycles. The switch is able to handle 20 dBm of RF power in both the ON and OFF-state. The power handling of the switch shows promising results but tests up to 30 dBm still need to be conducted.

Using two switches in parallel does allow for a reduction in R_{ON} without significantly diminishing F_{CO} . Splitting a switch into two parallel segments allows for a reduction in the voltage required to switch the device while only slightly increasing C_{OFF} and reducing the F_{CO} . The switch with the highest F_{CO} (9.6 THz) had an MPA of 1.32. This switch had 100 nm of GeTe with a 100 nm thick AlN barrier layer. This switch was 20 μm wide with a 1 μm wide heater and a 400 nm long RF gap. This switch takes advantage of the significant increase RF performance due reducing RF gap length and increasing GeTe thickness.

Chapter 6: Integration with RF CMOS Circuits

6.1 Abstract

This chapter presents *in-situ* reconfiguration of a CMOS inductor-capacitor voltage controlled oscillator (LC-VCO) and narrowband CMOS low noise amplifier (LNA) over two widely separated frequency bands using RF PC witches. The LC-VCO was reconfigured using a via style RF PC switch while the LNA was reconfigured using a 4-terminal RF PC switch. A special solder bump bonding process was used to bond externally fabricated CMOS chips with in-house fabricated PC switches. The bump bonding process developed had 100% bond yielded with minimal effect on the RF performance of the CMOS circuits. The presence of the solder bumps and PC switch in the 3/5 GHz LNA resulted in less than a 2 dB reduction in gain and a minimal increase in noise figure from 2 dB to 3 dB.

6.2 Introduction

Fabricating and testing standalone RF switches is important in order to isolate their electrical performance. However, to determine their viability in RF systems, they must be integrated with RF CMOS circuits. There are two ways in which the switches can be integrated with CMOS circuits: fabricating the switches directly on the CMOS chip or fabricating switches on a separate chip and then bump bonding them to the CMOS chip. In this work, the latter technique is used in an attempt to control the thermal environment of the switch during operation. As noted in a previous chapter, the cooling time of the switch is important to determine whether the PC-material can be amorphized. Additionally, fabricating the switch on a thermally conductive substrate, such as sapphire, is important in achieving fast cooling times. However, in CMOS, the top layers of the chip are comprised of SiO₂ and are microns thick in which, due to its low thermal conductivity (1 W/m-K), the cooling time would be too long to amorphize the switch. A thick, thermally conductive ($> 5 \mu\text{m}$), electrically insulating layer, such as AlN, needs to be added before the fabrication of the switch takes place. The individual CMOS chips are also

very small, less the 3 mm on each side, making them very difficult to handle. Fabricating switches on a separate wafer solves these problems but requires the CMOS chip to be bump bonded to a PC chip. This technique requires additional processing to both the PC chip and CMOS chip. This chapter will discuss the additional processing required to bump bond the chips together, the bonding process and any added steps that must be taken to ensure a functioning integrated chip. This chapter will also discuss the successful integration of RF PC switches with an LC VCO and an LNA.

6.3 Flip Chip Solder Bump Bonding Process

The first step is to build the solder bumps on the desired pads. The bumps consist of two layers: a Cu stud that is about 10 μm tall and 10 μm of Sn solder. The pads on the CMOS chip can be recessed as much as 4 μm into the top passivation layer of the chip (fig, 6.1). The Cu stud is used to act as a standoff between the CMOS chip and the PC chip, preventing the solder from reflowing into undesired places.

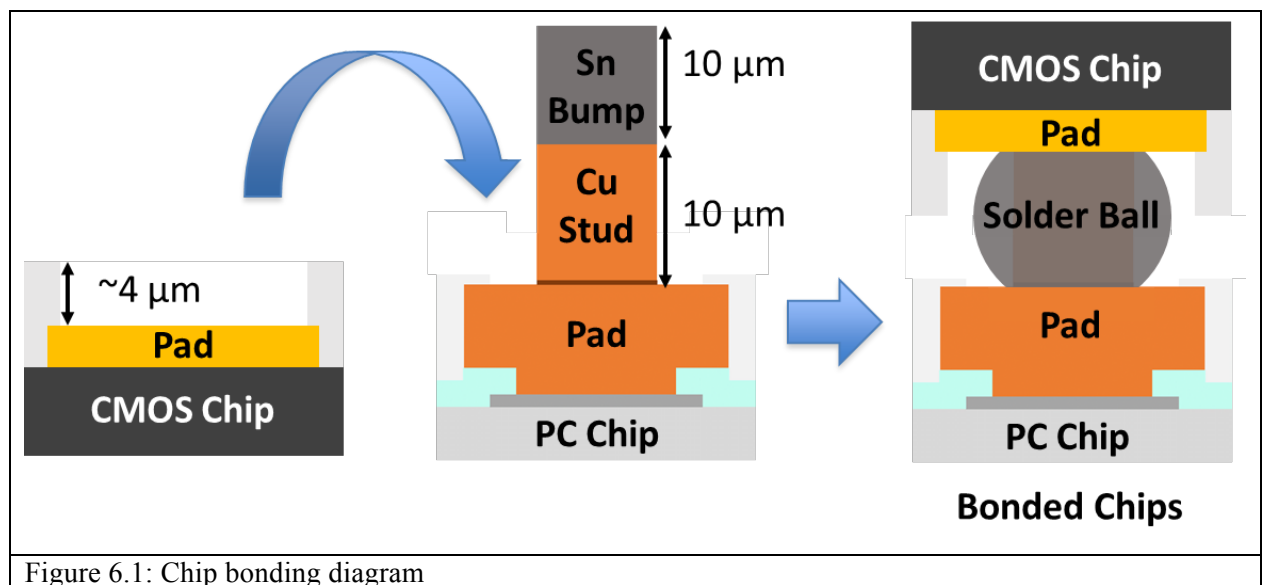
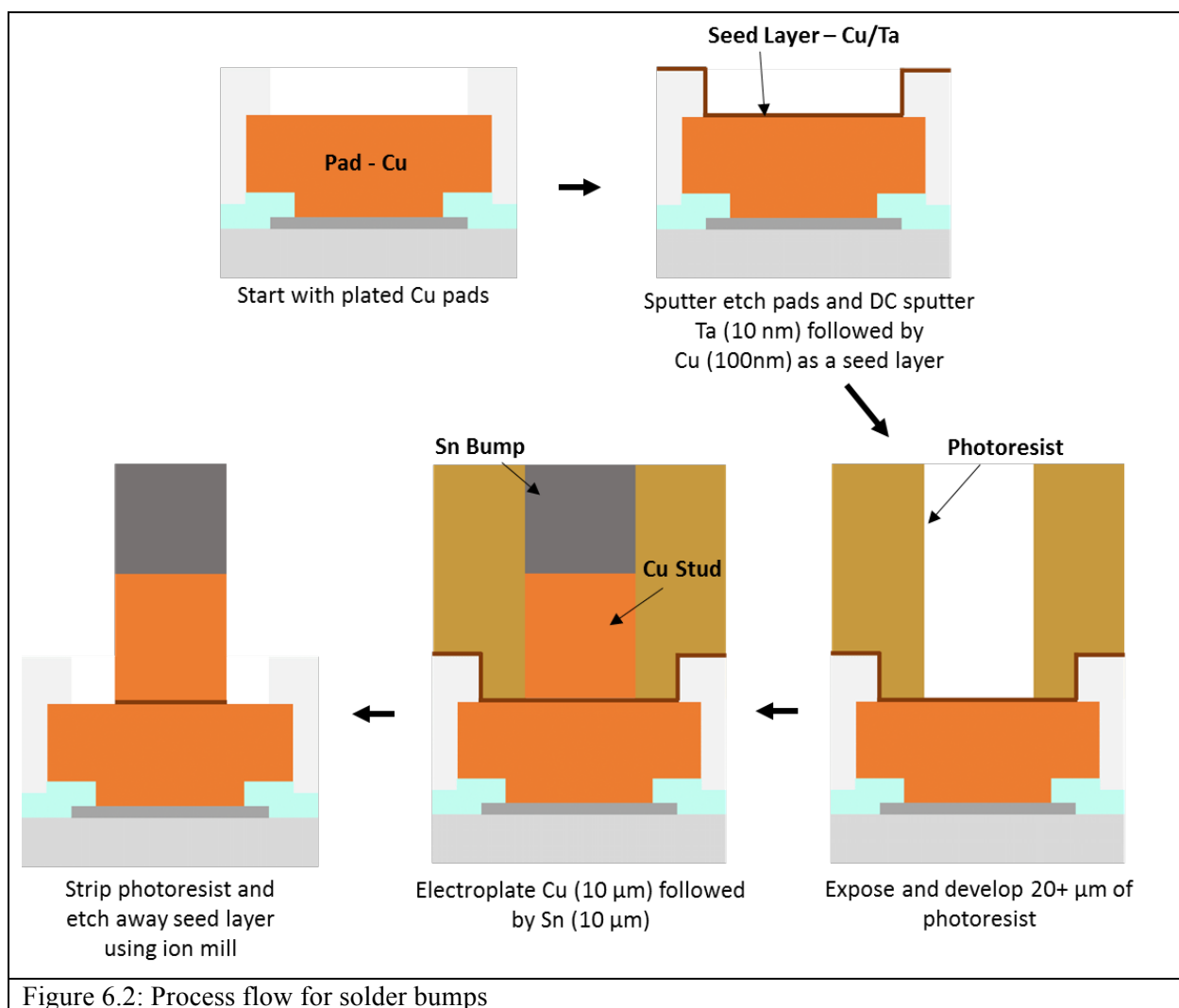


Figure 6.1: Chip bonding diagram

6.3.1 Solder Bump Process Flow

The process flow for the fabricating the solder bumps is shown in fig. 6.2. The first step is to deposit the Cu seed layer needed for electroplating the Cu studs and Sn bumps. This is done by first sputter etching the surface of the PC chip for 5 minutes to remove any oxide that might be present on the Cu pads, then depositing 10 nm of Ta followed by 100 nm of Cu using DC magnetron sputtering. After the seed layer is deposited, 20+ μm of photoresist is spun onto the PC chip using a double coating process. Circular windows are exposed over the Cu pads and the photoresist then is developed to create the plating mask for the Cu studs and Sn bumps. Next, a 1 minute O_2 descum in the parallel plater RIE is completed to remove any residual resist that may be present on the Cu pads where the electroplating is to take place. The sample is then placed in a Cu electroplating bath.



Using a pulsed power supply, with 15 ms of forward current and 1 ms of reverse current per pulse, for 100 minutes results in 10 μm of plated Cu. The sample is then transferred to the Sn plating bath. The same pulsed power supply settings are used to plate the Sn for 8 minutes yielding 10 μm of solder bumps. Once the plating is completed, the photo resist is stripped and the Cu/Ta seep layer is removed using an Ar^+ ion mill. Figure 3 shows the first generation of solder bumps after plating (fig. 6.3(a),(b)) and after reflow at 300 $^{\circ}\text{C}$ (fig. 6.3(c)). The solder bumps are 50 μm wide with a 100 μm pitch.

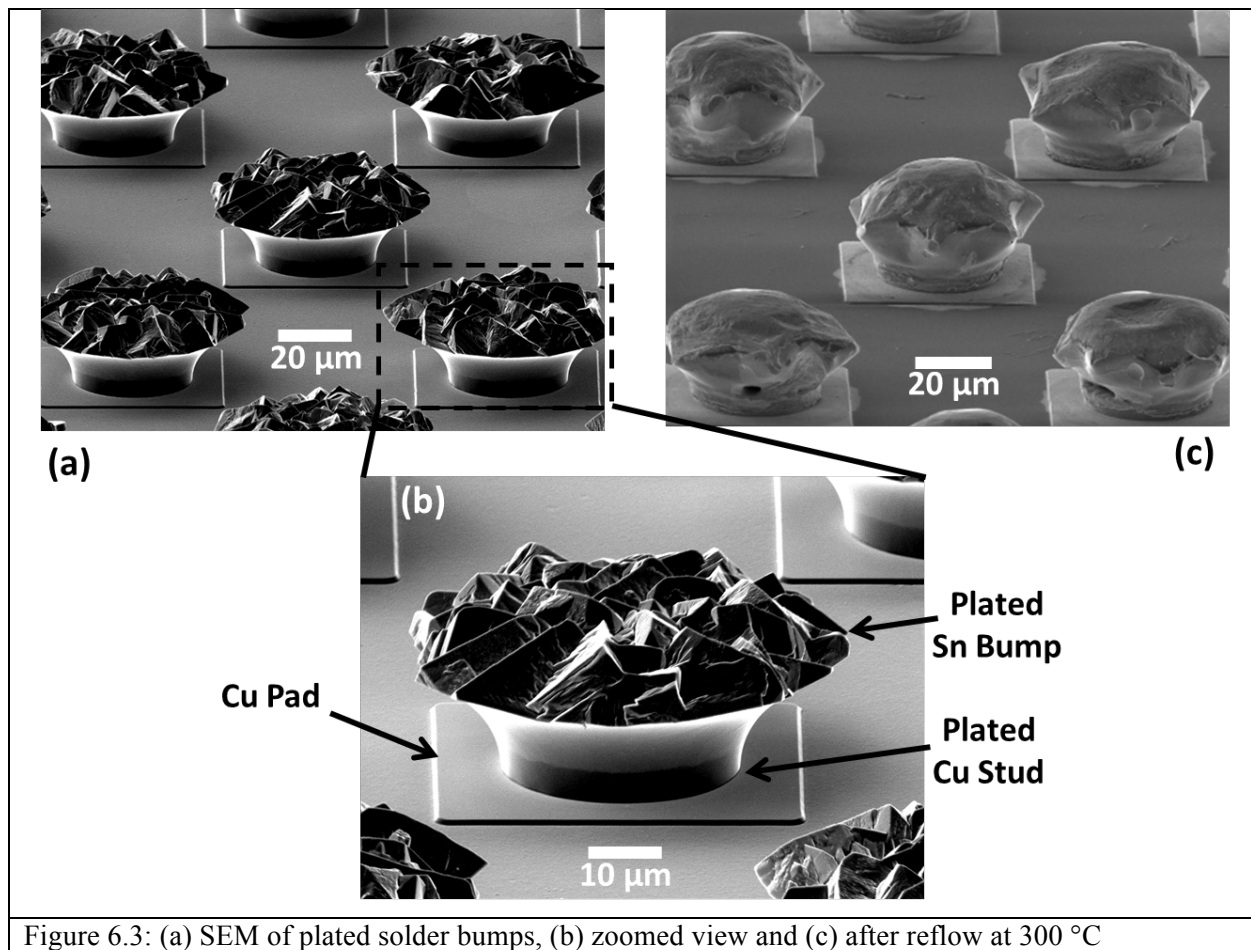


Figure 6.3: (a) SEM of plated solder bumps, (b) zoomed view and (c) after reflow at 300 $^{\circ}\text{C}$

6.3.2 CMOS Preparation

The CMOS chips also require post-processing before the bump bonding occurs because they arrive from the foundry with Al pads. The Sn solder bumps do not achieve adequate mechanical contact

with the Al pads and, therefore, Au must be deposited on the pads. An electroless Au plating process is used to deposit Au on to the Al pads. Au cannot be plated directly onto the Al. Therefore, Zn must be plated first which is followed by Ni plating. Finally, Au is plated onto the Ni. CMOS chips are first bonded to a 1 inch Si carrier wafer using photoresist for easier sample handling. The wafer is dipped in phosphoric acid for 30 seconds to remove any oxide that may have formed on the Al pads and is then rinsed with DI water. Next, Zn is electroless plated for 45 seconds at 40 °C. Then, the sample is desmuted using a 20% nitric acid solution for 15 seconds. More Zn is then plated, using a separate bath for 30 seconds also at 40 °C. After the second Zn layer is completed, the sample is rinsed with DI water and then placed in the electroless Ni plating solution at 90 °C for 10 minutes. The sample is then rinsed with DI water and placed in the Au electroplating bath at 70 °C for 10 minutes. Once the Au plating is completed, the sample is removed and then rinsed using DI water. It is carefully dried using compressed N₂. The individual CMOS chips are removed from the carrier wafer using acetone and IPA. The resulting Au film thickness is about 130 nm which is sufficient for bonding to take place.

The CMOS chips go through one last process before the bump bonding takes place. To ensure the solder bumps make good electrical and mechanical contact with the Au pads and Cu studs, solder flux is spun onto the CMOS chip. This is accomplished by mounting the CMOS chips using 90 °C heat release tape on a 1 inch Si carrier wafer. Then 5RMA liquid flux from INDIUM Corporation is spun onto the carrier wafer at 6000 RPM for 60 seconds. Once completed, the wafer is placed on 115 °C hotplate to release the CMOS chips.

6.3.3 Flip Chip Bonding

Once the solder bumps are plated onto the PC chip and the Au and solder flux is on the CMOS chip, both chips are ready to be bonded. The bonding takes place on a Laurie M flip chip die bonder.

The two chips are first aligned using an optical probe. Once alignment is complete, the optical probe is retracted and bonding can begin.

The bonding processes occurs in 4 steps. First, the two chips are pressed together with a force configuration of 1000 grams. Next, the chips are heated to 300 °C to melt the Sn bumps. Once the temperature of the chips reaches 300 °C, the force configuration is reduced to 115 grams. The chips are then cooled to room temperature while holding the force configuration constant at 115 grams. Once the bonding is complete, the bonded chips are soaked in acetic acid over night to remove any oxidation that may have occurred on the Cu pads that will be probed for testing.

6.4 LC-VCO

There have been two CMOS circuits that have been successfully integrated with PC switches using this solder bumping process that has been developed. The first was a reconfigurable LC VCO [4] that used three-terminal PC via switches (fig. 6.4). These switches were actuated by driving current directly through the PC-material to induce joule heating in the via. The PC switches were used to change the inductance seen by the VCO. The bonded chips can be seen in fig. 4. The solder bumps were on 100 μm wide Cu pads that were spaced 150 μm apart. The reconfigurable LC VCO was able to oscillate when powered. This demonstrates that the solder bumping process was successful with a 100% solder bump yield. The performance of the VCO can be seen in C. Wen et al. [4].

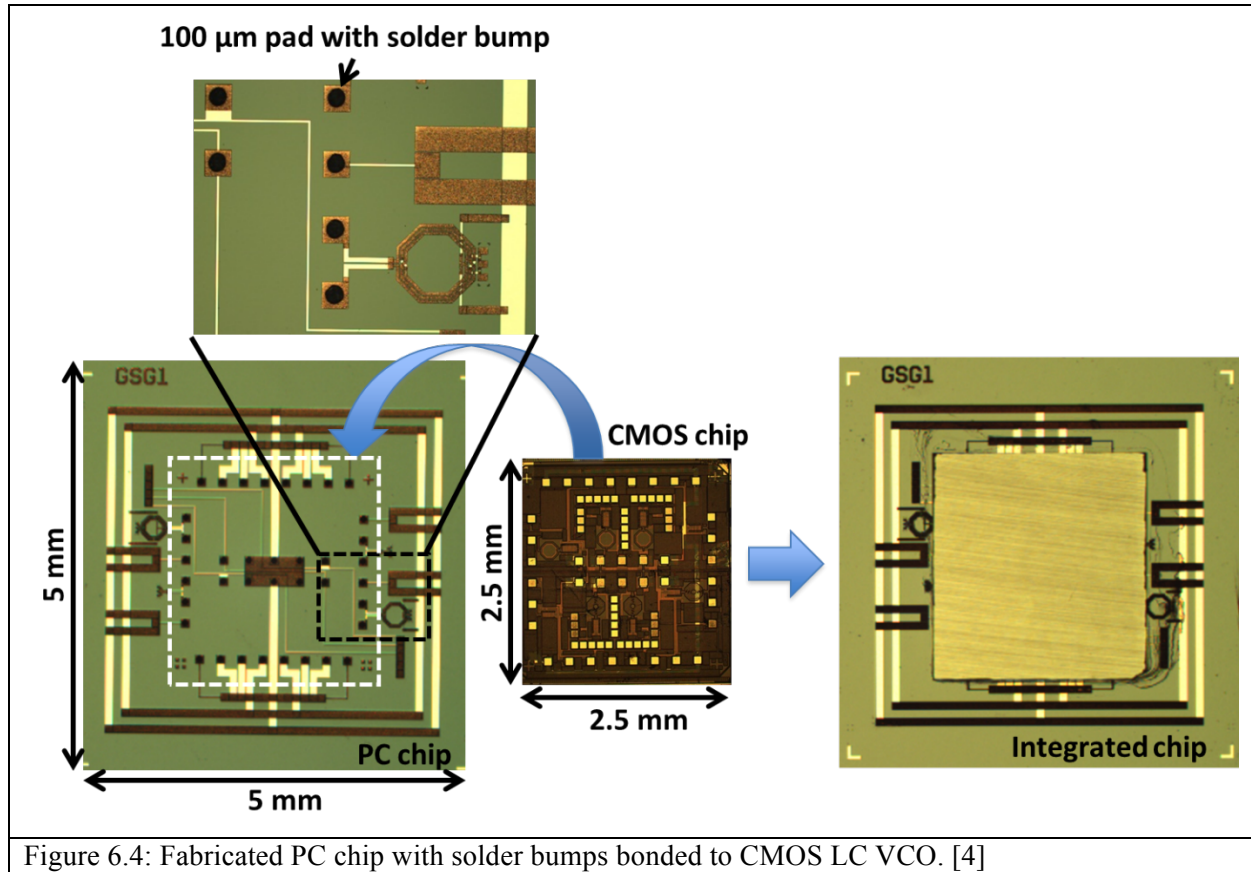


Figure 6.4: Fabricated PC chip with solder bumps bonded to CMOS LC VCO. [4]

6.5 3/5 GHz LNA

6.5.1 Switches Fabricated

A 3/5 GHz reconfigurable LNA was also integrated with a single phase change switch (fig. 6.5) [8] using the solder bumping process. A 4-terminal inline RF PC switch was used to switch between the 3 and 5 GHz modes of the LNA. Two CMOS LNAs were bonded to two different PC chips. The PC chip included a PC switch as well as power supply voltage lines and control voltage lines that required electrical connections to the CMOS chip. Two control samples were also bonded to CMOS LNAs where the PC switch is replaced with an ideal open switch or ideal short switch. For the ideal open switch, the PC-material and Au metallization layers are removed while, for the ideal short switch, the PC-material is replaced with Au. These control samples were used to determine the effect of the solder bumps on the

LNA's performance. Due to the smaller width of the CMOS chip and the greater number of pads needed, the size of the solder bumps had to be reduced to $50\text{ }\mu\text{m}$ with a $50\text{ }\mu\text{m}$ spacing.

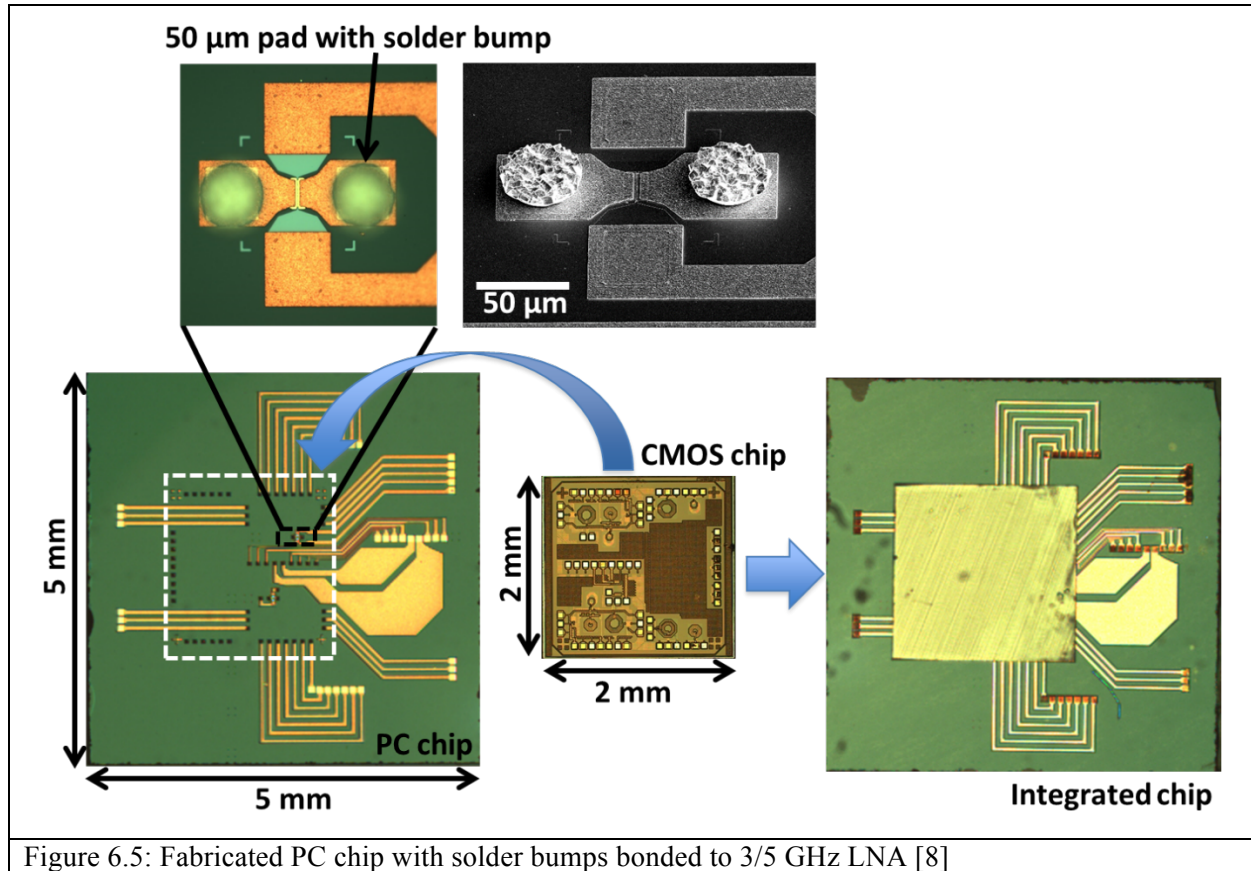
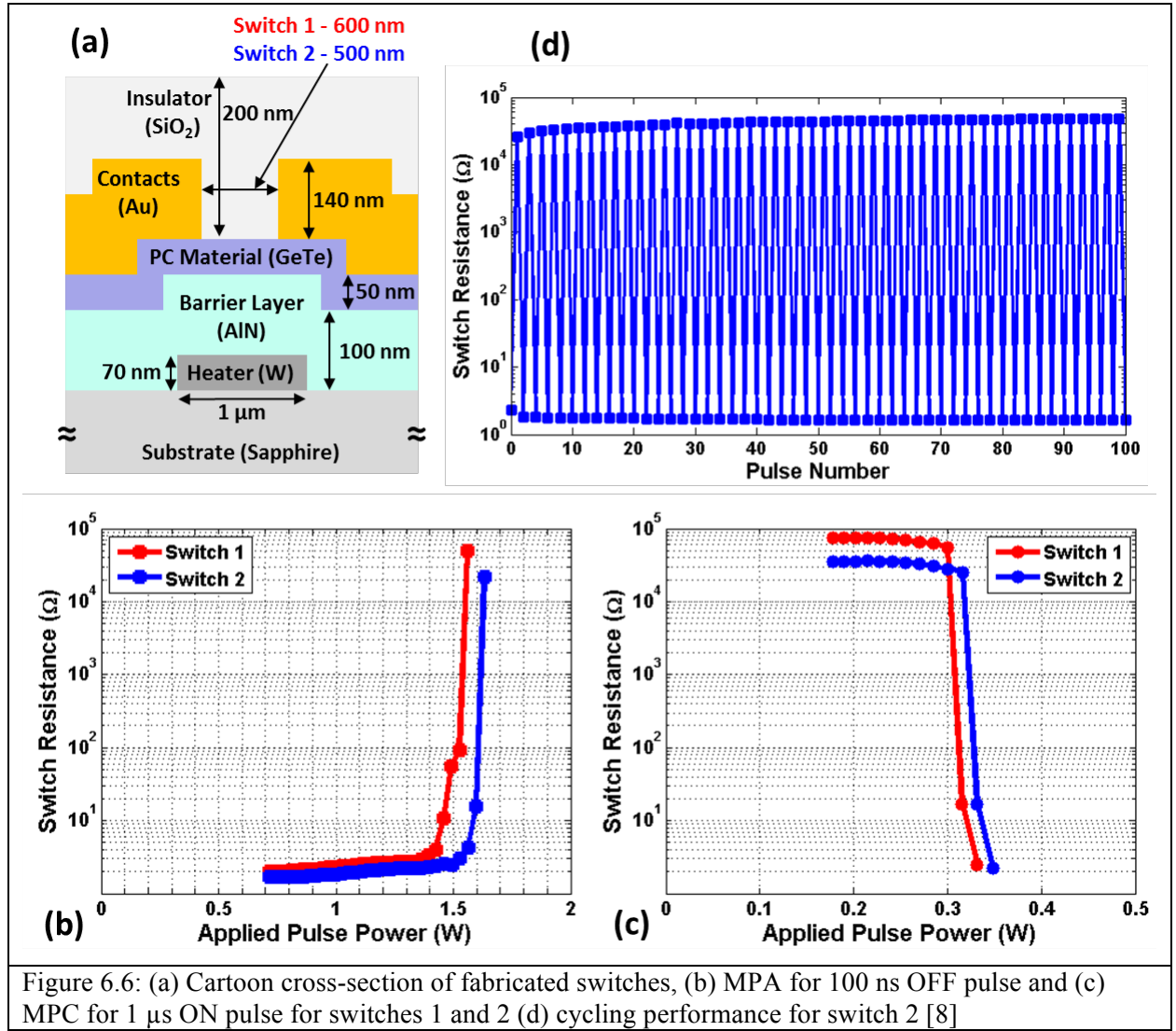


Figure 6.5: Fabricated PC chip with solder bumps bonded to 3/5 GHz LNA [8]

6.5.2 Standalone Switch Measurements

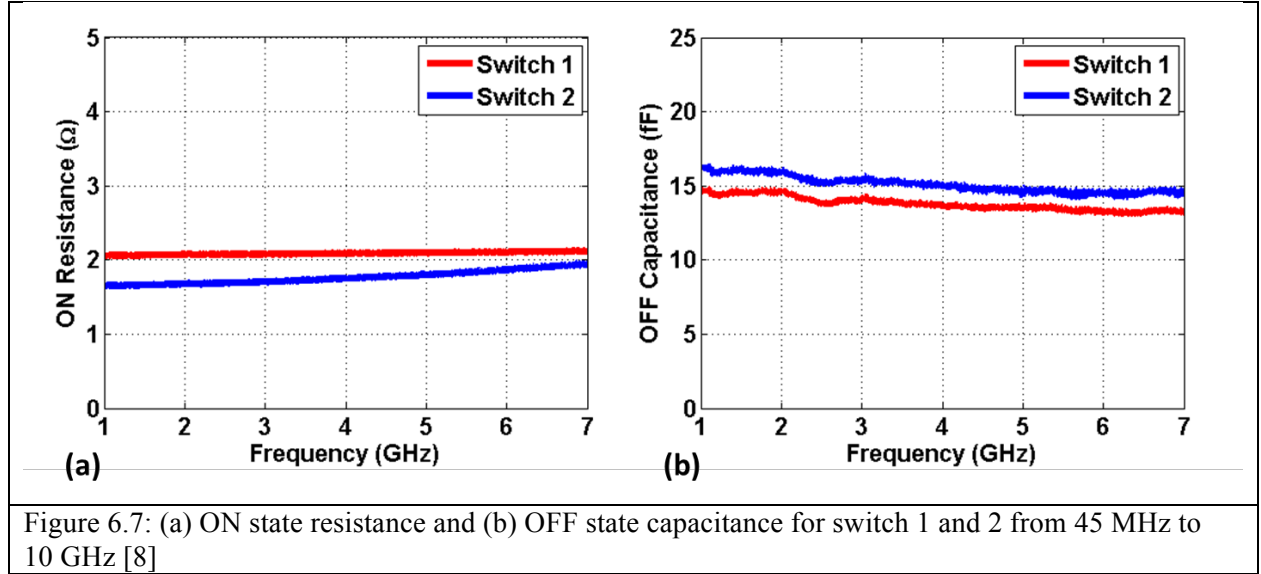
The two standard $20\text{ }\mu\text{m}$ wide switches with different RF gap lengths were integrated with the CMOS LNA. Switch 1 had an RF gap length of 600 nm while switch 2 had an RF gap length of 500 nm (fig. 6.6(a)). The MPA, MPC, cyclability and RF properties of similar standalone switches were measured on the same fabricated wafer. The resistance of both heaters was $39\text{ }\Omega$. The initial resistance of switch 1 was $2.0\text{ }\Omega$ and, for switch 2, the resistance was $1.7\text{ }\Omega$. The difference in resistance was to be expected due to switch 2 having a shorter RF gap, which resulted a slightly higher MPA of 1.62 W

compared to 1.56 W for switch 1 (fig. 6.6(b)). The MPC was 0.33 W and 0.35 W for switches 1 and 2, respectively. Switch 2 was pulsed 100 times between the ON and OFF state (fig. 6.6(d)), using a 100 ns long OFF pulse at 9.2 V (1.7 W) and a 1 μ s long ON pulse at 4.4 V (0.38 W).



RF measurements were also made on standalone devices similar to switches 1 and 2 that were bonded to the LNA. Using the VNA, 1-port measurements were made with the switches in both the ON and OFF state. Using the de-embedding techniques discussed in an earlier chapter, R_{ON} (fig. 6.7(a)) and

C_{OFF} (fig. (6.7(b))) were measured from 1 GHz to 7 GHz, which covers both bands of operation in the LNA. The ON state resistance was $2.1\ \Omega$ and $1.6\ \Omega$ for switches 1 and 2, respectively. The OFF state capacitance was 13.8 fF and 15.5 fF for switches 1 and 2, respectively. This resulted in an F_{CO} of 5.5 THz for switch 1 and 6.4 THz for switch 2.



6.5.3 LNA Performance

In conjunction with Rahul Singh, S_{21} and noise figure measurements (NF) were made on 6 different LNAs (fig. 6.8). When the switch is “ON” or shorted, the LNA operates in the 3 GHz mode. When the switch is “OFF” or open, the LNA operated in the 5 GHz mode. Each mode of operation was measured of three different circuit setups: CMOS only, ideal short/open switches and RF PC switches. The CMOS only measurements were made directly on the CMOS LNA without it being bump bonded to another chip. For the short-open measurements, a CMOS LNA was bump bonded to a chip where Au replaced the PC material in the switch to act as an ideal short switch and another where the PC material was completely removed to act as an ideal open switch. The other two LNAs were bump bonded to PC switch 1 (600 nm RF gap) and switch 2 (500 nm RF Gap).

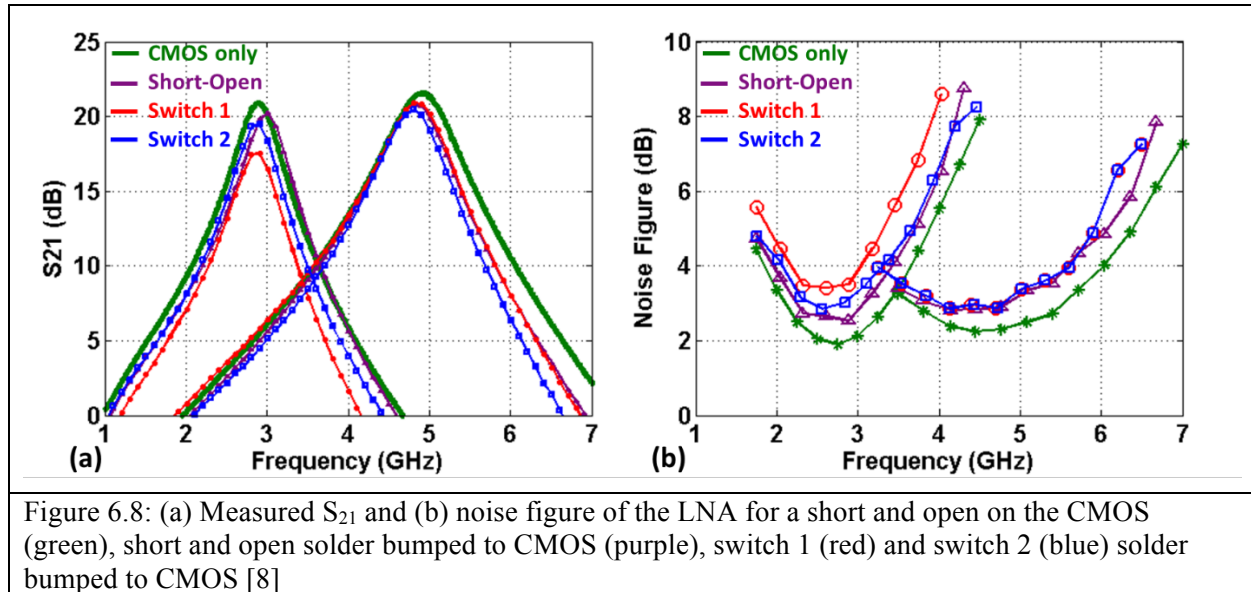
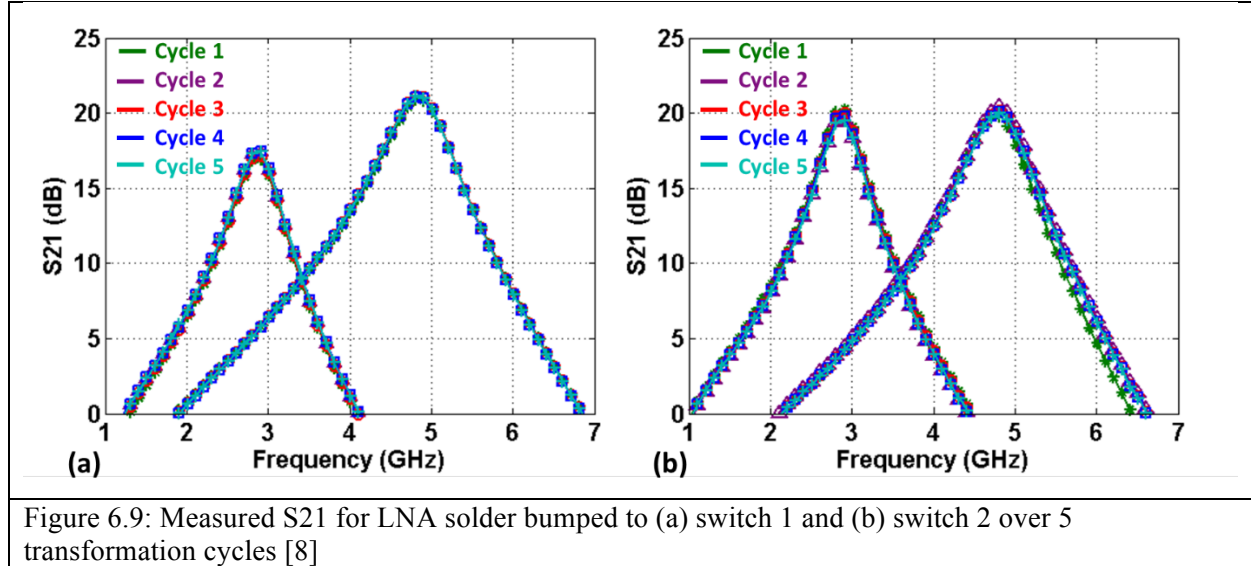


Figure 6.8: (a) Measured S_{21} and (b) noise figure of the LNA for a short and open on the CMOS (green), short and open solder bumped to CMOS (purple), switch 1 (red) and switch 2 (blue) solder bumped to CMOS [8]

The measured S_{21} of the LNA does not seem to be affected by the addition of the solder bumps. The maximum gain is 20.6 dB in the 3 GHz mode and 21.6 dB in the 5 GHz mode when measured directly on the CMOS LNA. When measured on the LNAs bump bonded to an ideal short and open switch, the gain reduces slightly to 20.2 dB and to 20.55 dB for the 3 and 5 GHz modes, respectively. The addition of the solder bumps appears to have more impact on the noise figure of the LNA than on the gain. The noise figure increases from 1.9 dB to 2.55 dB in the 3 GHz mode and from 2.25 dB to 2.8 dB in the 5 GHz mode. However, the increase in the noise figure is modest and the solder bumping process contributes minimal performance degradation to the reconfigurable LNA.

When the PC switches replace the ideal short and open switch, the performance of the LNA in the 3 GHz mode suffers more than in the 5 GHz mode. In the 3 GHz mode, the gain is 17.5 dB for switch 1 and 19.5 dB for switch 2 with respective noise figures of 3.41 dB and 2.85 dB. For the 5 GHz mode, the gain is 20.9 dB and 20.1 dB for switches 1 and 2, respectively, which is within 0.7 dB of the gain for the LNA bonded to an ideal open switch. The noise figure in the 5 GHz mode for switches 1 and 2 is 2.86 dB which is within 0.1 dB of the noise figure for the ideal open switch. This suggests that the OFF state capacitance has less of an impact on the performance of the LNA than does the ON state resistance. The

reduction in S_{21} for switch 1 in the 3 GHz mode is probably due to increased contact resistance between the solder bumps and the aluminum bond pads on the CMOS chip due to a weak solder joint. Both switches were also cycled on and off 5 times while the S_{21} of the LNA was measured after the switches were turned off and then again after they were turned back on (fig. 6.9). The gain of the LNA in both modes was not affected by the cycling of the switch.



A summary of the measurements result of the LAN are shown in table 6.1. The effect of the PC switch and solder bumps can be most clearly seen while analyzing the NF of the LNA when the switch is in the ON-state (3 GHz Mode). The addition of the solder bumps results in a 0.65 dB increase in NF while the PC switch only increases the NF by 0.3 dB. This shows that a fully integrated switch directly on the CMOS circuit would result in a NF of no more than 2.2 dB.

	3 GHz Mode (Switch ON)		5 GHz Mode (Switch OFF)	
	S_{21} (dB)	NF (dB)	S_{21} (dB)	NF (dB)
CMOS Only	20.6	1.90	21.6	2.25
Bonded Chip	20.2	2.55	20.8	2.80
Bonded Chip with PC 1	17.5	3.41	20.9	2.86
Bonded Chip with PC 2	19.5	2.85	20.1	2.86

Table 6.1: Summary of LNA performance [8]

6.6 Summary

Measuring the performance of a standalone RF switch is important, but its true impact cannot be determined until it is successfully integrated with RF circuits to achieve the reconfigurability that otherwise would not be possible. Using a solder bump bonding process, fabricated RF PC switches have been successfully integrated with RF CMOS circuits. The solder bump process has a 100% bonding yield and contributes minimal performance degradation to the RF circuit. A reconfigurable LNA that has the ability to operate at both 3 GHz and 5 GHz using a single 4-terminal inline RF phase change switch has been demonstrated, while simultaneously achieving the RF performance of non-reconfigurable CMOS circuits. The addition of a bonded chip with a PC switch resulted in a 0.65 increase in NF from the bonding and only 0.3 dB from the switch in the 3 GHz mode. This illustrates the promise of these switches as an enabling technology for complex field-programmable transceivers. The reconfigurability would not be possible using traditional RF CMOS technology.

Chapter 7: Conclusions and Outlook

7.1 Conclusions

This thesis detailed the design and performance of a 4-terminal RF PC switch for use in reconfigurable RR circuits. A 3-D model of the switch was developed and its validity was established by comparing it to measured results. In order to ensure the model's accuracy, it included the temperature dependent thermal conductivity and heat capacity of the sapphire substrate. A thermal interface conductance of $200 \text{ MW/m}^2\text{-K}$ between the W heater and the sapphire substrate as well as the TCR of the W heater were also included in the model to improve accuracy. Using a 2-D model, the F_{CO} of the switch was shown to double by reducing the RF gap length from 900 nm to 100 nm. The simulations also showed that increasing the heater width had no performance benefits due to a reduction in F_{CO} with an increase in MPA. The use of a notch in the GeTe for a 100 nm long RF gap was shown to reduce the MPA more effectively than increasing the RF gap length.

Three major contributions have been achieved regarding the materials used in the PC switch. The introduction of low resistivity W for the heater, AlN for the barrier layer, and low resistivity GeTe have the ability to double the F_{CO} /MPA ratio. Low resistivity W ($72 \text{ n}\Omega\text{-m}$) allows for a reduction of voltage required to switch the device as well as increased heater reliability when compared to a NiCrSi heater (18.6 V for NiCrSi and 8.4 V for W). The inclusion of AlN barrier layer enables an increase in electrical isolation of the heater from the RF signal path while still maintaining the desired thermal coupling to the PC layer. The use of co-deposition from elemental Ge and Te targets onto a heated substrate allowed for a reduction in GeTe resistivity from $3 \text{ }\mu\Omega\text{-m}$ to $1.5 \text{ }\mu\Omega\text{-m}$. This single improvement in GeTe resistivity will enable a doubling in RF performance.

DC and RF measurements were taken on an array of switches with varied switch width, heater width, RF gap length, AlN thickness and GeTe thickness. Increasing the GeTe thickness from 50 nm to 100 nm reduces R_{ON} without increasing the MPA. Reducing the RF gap length also increases the F_{CO} of

the switch with minimal increases in MPA. Increasing the AlN thickness from 105 nm to 170 nm does reduce the OFF-state capacitance of the switch from 15 fF to 10 fF, with only a 14% increase in MPA. However, increasing the AlN thickness even further, to 200 nm, did not cause any further reduction in C_{OFF} , thereby leading to the conclusion that a 20 μm wide switch cannot have a capacitance less than 10 fF. Of that 10 fF of capacitance, 3.7 fF is attributed to the fringing capacitance from switch to the heater pads. The remaining capacitance is due to the contact metallization.

Increasing the width of the heater only increases the MPA and C_{OFF} of the switch. Therefore, it is a design feature that should be minimized. Increasing the switch width does increase its F_{CO} ; however, this effect is not as substantial as reducing the RF gap length and increasing the GeTe thickness. The use of two 10 μm wide switches in parallel allowed for a significant reduction in the voltage required to transform the switch with only a slight increase in C_{OFF} . The ability to reduce the voltage requirements of the switch is necessary to allow the heaters to be driven with on-chip CMOS circuitry instead of by an external pulse generator.

The fabricated switches demonstrated promising power handling capabilities. Switches in both the ON and OFF-state were able to withstand 20 dBm of RF power without effecting the switches' RF performance. Cycling of the switch (5 cycles) also did not affect the RF performance of the switch. However, when the switch was cycled (99 cycles) using DC measurements only, the R_{ON} of the switch began to increase after 50 cycles. The R_{ON} of the switch went from 1.7 Ω to almost 5 Ω at the end of 99 cycles.

The integration of these switches into a reconfigurable 3/5 GHz LNA, using a special solder bump bonding process that was developed specifically for use in this application, was also demonstrated. The addition of the switch or the solder bumps did not degrade the RF performance of the LNA. This demonstrates that this RF switch technology can be stably and reversibly reconfigured to achieve wideband functionality while maintaining the RF performance of narrowband non-reconfigurable CMOS

circuits. The addition of the solder bumps results in a 0.65 dB increase in NF while the PC switch only increases the NF by 0.3 dB in the 3 GHz mode when the switch is in the ON-state.

7.2 Future Work

Despite all of the advancements in RF PC switch performance that this research has developed and demonstrated, there is still more work to be done. An explanation regarding the reasons for the resistivity of the GeTe in the switch differs from sheet film measurements is needed. If the resistivity of the GeTe in the switch can be reduced to the $1.5 \mu\Omega\text{-m}$ measured on sheet films, the R_{ON} of the switch has the potential to drop in half. Reducing the contact resistance to the GeTe is also important to allow for further reductions in R_{ON} . Using another contact metal such as Ni may lead to lower contact resistance as well as improve cyclability of the switch.

Monolithic integration of this switch into a backend CMOS process is required to ensure its viability as a future technology. There are currently two major obstacles that must be overcome in order to achieve full integration with CMOS circuits. The first is that the thermal environment of the switch must be improved. There is approximately $10 \mu\text{m}$ of SiO_2 on top of the Si substrate. Building a PC switch on that much oxide would not be possible. The cooling time of the switch would be too long and the switch could never be turned off. A thick thermally conductive layer, such as AlN, on top of the SiO_2 must be present to act as a thermal ground for the switch. This would allow for the decrease in cooling time needed to amorphize the PC material. The required thickness of AlN needed should be simulated to determine its viability and be experimentally verified. The voltage required to amorphize the switch must also be reduced if the heater is to be driven using CMOS circuitry. There are a number of ways this can be accomplished. The first method would be to increase the efficiency of the heating of the PC material by patterning the AlN layer. By having the AlN only on top of the heater and back filling the rest of the region with SiO_2 , the AlN would act as a heat funnel while the SiO_2 would prevent lateral heat spreading.

This not only reduces the power and voltage required to switch the device, but would also decrease the cooling time of the switch by reducing the volume of material that is heated. The thickness of the heater should also be increased to reduce its resistance, thereby reducing the voltage needed to reach the same power. Splitting the switch into multiple parallel segments would also reduce the effective heater resistance. Using all of these techniques should enable on-chip reconfiguration capabilities that have never been accomplished before.

The power handling capabilities of these RF switches must also be further examined. Current tests show promising results up to 20 dBm of incident power but, due to the limitations of the instrumentation used, higher powers could not be tested. The ability to hold up to 30 dBm of incident power is needed if these switches are to be used in power amplifier applications. The use of switches in series and parallel combinations could allow for increased power handling capabilities without sacrificing RF performance.

This 4-terminal RF PC switch has the capacity to revolutionize reconfigurable RF circuits. Its ability to have sub $1\ \Omega$ resistance in the ON-state and electrically decouple the programming signal from the RF signal path uniquely positions this switch technology for reconfigurable RF applications. It is not unreasonable to think this switch technology could be present in every new cellphone manufactured within the next 5 to 10 years.

7.3 Contributions and Publications

This section will outline the publication, both submitted and in-progress, along with their contributions that arose from the work discussed in this thesis.

1. AlN Barriers for Capacitance Reduction in Phase-Change RF Switches

Electron Device Letters

– In review

- a. First introduction of AlN as the barrier layer in an RF PC switch
- b. Outlines the benefits of AlN over SiN_x for both reducing MPA and heater temperature for a given F_{CO} using simulations
- c. Shows the reduction in C_{OFF} from 15 fF to 10 fF increasing the AlN barrier layer thickness from 105 nm to 170 nm
- d. Uses simulation results to demonstrate the increase in MPA from making the AlN barrier layer thicker is due to an increase in thermal capacitance and not an increase in thermal impedance due to the additional AlN

2. Design and Optimization of Phase-Change RF Switches

Transactions on Microwave Theory and Techniques

- In preparation

- a. Outlines the benefits of reducing the RF gap length by showing an increasing in F_{CO} /MPA for shorter RF gaps
- b. Shows that reducing the heater width reduces the MPA while increasing the switch F_{CO} and extrapolating to a “0” width heater
- c. Compare C_{OFF} for different width switches to determine the fringing capacitance of the switch and how much capacitance is contributed by the metal contacts and how much is contributed by the heater

- d. Show the effect of increasing the AlN to 200 nm on C_{OFF} and that the capacitance attributed by the heater has disappeared
- e. Corroborate the previous results with the insertion-loss of a grounded heater for both 100 nm and 200 nm of AlN
- f. Outline the path for scaling the device to allow for CMOS driven heaters and that segmented switches are the solution and show an example of a segmented switch

3. Reliability of Tungsten Micro-Heaters for use in RF Phase-Change Switches

Electron Device Letters

- Final stages of data collection

- a. Show the effect of heated W deposition on both resistivity and TCR for deposition temperatures of 25° C, 400° C and 850° C
- b. Use simulations to show that reducing the W resistivity is critical to reducing the voltage required to amorphize the PC material
- c. Show the XRD data for all three deposition temperatures of W
- d. Show heater reliability data of all three W films for different heater lengths and widths – still need to be measured
- e. Conclude that the increase in deposition temperature results in more durable heaters
- f. Conclude that longer heaters are more fragile

4. Developing Low Resistivity GeTe films for RF Phase-Change Switches

Journal of Vacuum Science and Technology B

- Final stages of data collection

- a. Detail the process used for reducing the resistivity of the GeTe to 1.5 $\mu\Omega\cdot\text{m}$
- b. Show the resistivity and RMS roughness dependence on deposition temperature – still needs to be measured for a complete set of films
- c. Show resistivity as a function of composition – may need the RBS or other technique to determine the composition of the films

- d. Outline the importance of reducing the resistivity of the GeTe on both F_{CO} and MPA
5. A 3/5 GHz Reconfigurable CMOS Low-Noise Amplifier Integrated with a Four-Terminal Phase-Change RF Switch
 R. Singh, G. Slovin, M. Xu, A. Khairi, S. Kundu, T. E. Schlesinger, J. A. Bain, and J. Paramesh
 International Electron Device Meetings – 2015
 - a. Demonstrated reconfigurable 3/5 GHz CMOS LNA using an RF PC switch
 - b. Showed solder bumping process introduced greatest degradation in noise figure of 0.6 dB
 - c. Showed RF PC switch only introduce 0.3 dB degradation in noise figure
 - d. Amplifier gain was unaffected by the presence of the switch in both the ON and OFF-state
 - e. Amplifier gain was unaffected by cycling the switch between the ON and OFF-state five times
 6. A Phase-Change Via-Reconfigurable CMOS LC VCO
 C.-Y. Wen, G. Slovin, J. A. Bain, T. E. Schlesinger, L. T. Pileggi, and J. Paramesh
 IEEE Trans. Electron Devices, vol. 60, no. 12, pp. 3979–3988, 2013
 - a. Demonstrated reconfigurable LC VCO using via-style RF PC switch
 - b. Via-style switch was used to tune inductors to allow for a wider tuning range VCO
 7. A process for transferring and patterning InAs quantum dot optical gain media for HAMR near field optical sources
 E. B. Quirk, A. Gamble, R. Hussin, G. Slovin, Y. Kong, T. E. Schlesinger, J. A. Bain, K. Kuriyama, and Y. Luo
 IEEE Trans. Magn., vol. 49, no. 7, pp. 3564–3567, 2013
 - a. Not related to this work and was a side project

Appendix

Detailed process flow for standard switch and solder bumps

Sapphire Substrate Cleaning

8. Ultrasonic substrates in acetone of 10 minutes
9. Rinse with IPA and dry with N₂
10. IPC barrel etch in O₂ at 1 Torr for 1 minute with 100 W of RF power

Deposit W in AJA

1. Preheat the substrate at 850° C for 5 minutes
2. Pre-sputter W at 3 mTorr (60 sccm Ar) for 10 minutes with 50 W of DC Power
3. Deposit W at 3 mTorr (60 sccm Ar) for 1800 seconds with 50 W of DC Power ~ 70 nm

Pattern W Heater

1. Clean sample with acetone, IPA and N₂ dry
2. HMDS of #4 10 minute vapor prime at 150° C
3. Spin coat AZ4110 at 4000 RPM for 60 seconds
4. Bake on 95° C hotplate for 2 minutes
5. Expose photoresist for 20 seconds with an exposure density of 5 mW/cm²
6. Develop in AZ4000K 1:4 for 2.5 to 3 minutes
7. Flood expose resist for 70 seconds with an exposure density of 5 mW/cm²
8. Etch W in Plasma -Therm Parallel Plate RIE
 - a. CHF₃ 22.5 SCCM
 - b. O₂ 16 SCCM
 - c. 100 mTorr
 - d. 100 W RF (~350 V bias)

- e. 6 minutes
- 9. Soften photoresist in IPC barrel etcher with O₂ at 1 Torr for 3 minute with 200 W of RF power
- 10. Ultrasonic sample for 10 minutes in acetone
- 11. Rinse with IPA and dry with N₂

Despite AlN in Tegal

- 1. Sputter etch substrate at 15 SCCM Ar for 1 minute at 100 W RF power
- 2. Reactive sputter Al
 - a. Ar 23 SCCM
 - b. N₂ 32 SCCM
 - c. 7 kW AC power
 - d. 300 W DC power
 - e. 80 seconds ~ 100 nm

Deposit GeTe in AJA

- 1. Preheat the substrate at 160° C for 5 minutes
- 2. Sputter etch substrate at 3 mTorr (60 sccm Ar) for 1 minutes at 50 W RF power
- 3. Pre-sputter at 3 mTorr (60 sccm Ar) for 5 minutes with Ge at 35 W DC and Te at 25 W RF power
- 4. Deposit at 3 mTorr (60 sccm Ar) for 415 seconds with Ge at 35 W DC and Te at 25 W RF power
~50 nm

Pattern GeTe

- 1. Clean sample with acetone, IPA and N₂ dry
- 2. HMDS of #4 10 minute vapor prime at 150° C
- 3. Spin coat AZ4110 at 4000 RPM for 60 seconds
- 4. Bake on 95° C hotplate for 2 minutes
- 5. Expose photoresist for 20 seconds with an exposure density of 5 mW/cm²

6. Develop in AZ Developer 1:1 for 3 to 3.5 minutes
7. Etch in Commonwealth Scientific Ion Mill (Hazardous)
 - a. Ar 1.2×10^{-4} Torr (~ 4 SCCM)
 - b. Wait 30+ minutes for gas pressure to stabilize
 - c. 10 mA and 500 V
 - d. When neutralizing current is on -1 mA
 - e. 4 minutes
8. Soften photoresist in IPC barrel etcher with O₂ at 1 Torr for 3 minute with 200 W of RF power
9. Ultrasonic sample for 10 minutes in acetone
10. Rinse with IPA and dry with N₂

Contacts E-Beam Patterning

1. Spin coat PMMA A7 at 1000 RPM for 90 seconds
2. Bake on 150° C hotplate for 2 minutes
3. Deposit ~ 10 nm of AlSiCu in CVC
 - a. 5 mTorr 50 SCCM Ar
 - b. 250 W DC power
 - c. 25 seconds
4. Expose patterns using FEI Sirion 400 SEM / JC Nability NPGS E-Beam Lithography
 - a. Spot size 1 (25-30 pA)
 - b. $300 \mu\text{C}/\text{cm}^2$
 - c. Mag 1700x
 - d. Center to Center and Line to Line Spacing of ~ 8 nm
5. Strip AlSiCu by dipping in AZ400K 1:3 for 30 seconds
6. DI rinse and N₂ dry
7. Develop in MIBK:IPA 1:3 for 60 seconds

8. Dip in IPA for 15 seconds
9. N₂ Dry
10. Descum in IPC barrel etch with O₂ at 1 Torr for 2 minute with 100 W of RF power

Deposit W/Au contacts in AJA

1. Sputter etch substrate at 3 mTorr (60 sccm Ar) for 1-3 minutes at 50 W RF power
2. Pre-sputter W at 3 mTorr (60 sccm Ar) for 10 minutes with 50 W of DC power
3. Deposit W at 3 mTorr (60 sccm Ar) for 300 seconds with 50 W of DC power ~10 nm
4. Deposit Au at 3 mTorr (60 sccm Ar) for 1600 seconds with 50 W of DC power ~130 nm
5. Ultrasonic sample in acetone for 10 minutes or until liftoff is complete
6. Rinse with IPA and N₂ dry

Deposit SiO₂ in AJA

1. Pre-sputter SiO₂ at 3 mTorr (60 sccm Ar) for 5 minutes with 250 W of RF power
2. Deposit SiO₂ at 3 mTorr (60 sccm Ar) for 3105 seconds with 250 W of RF power ~100 nm

Pattern Vias in SiO₂

1. Clean sample with acetone, IPA and N₂ dry
2. HMDS of #4 10 minute vapor prime at 150° C
3. Spin coat AZ4110 at 4000 RPM for 60 seconds
4. Bake on 95° C hotplate for 2 minutes
5. Expose photoresist for 25 seconds with an exposure density of 5 mW/cm²
6. Develop in AZ4000K 1:4 for 2.5 to 3 minutes
7. Etch SiO₂ in Plasma -Therm Parallel Plate RIE
 - a. CHF₃ 22.5 SCCM
 - b. O₂ 16 SCCM
 - c. 100 mTorr

- d. 100 W RF (~350 V bias)
 - e. 2.5 minutes
- 8. Soften photoresist in IPC barrel etcher with O₂ at 1 Torr for 3 minute with 200 W of RF power
- 9. Ultrasonic sample for 10 minutes in acetone
- 10. Rinse with IPA and dry with N₂

Pattern Vias in AlN

- 1. Clean sample with acetone, IPA and N₂ dry
- 2. HMDS of #4 10 minute vapor prime at 150° C
- 3. Spin coat AZ4110 at 4000 RPM for 60 seconds
- 4. Bake on 95° C hotplate for 2 minutes
- 5. Expose photoresist for 25 seconds with an exposure density of 5 mW/cm²
- 6. Develop in AZ4000K 1:4 for 2.5 to 3 minutes
- 7. Etch AlN in Plasma -Therm ICP Versaline RIE
 - a. Cl₂ 25 SCCM
 - b. BCl₃ 5 SCCM
 - c. Ar 70 SCCM
 - d. 5 mTorr
 - e. 100 W ICP power
 - f. 30 W bias power
 - g. 150 seconds
- 8. Soften photoresist in IPC barrel etcher with O₂ at 1 Torr for 3 minute with 200 W of RF power
- 9. Ultrasonic sample for 10 minutes in acetone
- 10. Rinse with IPA and dry with N₂

Electroplate Cu pads and traces

1. Deposit Cu seed layer in CVC
 - a. Sputter etch sample at 5 mT (50 SCCM Ar) for 3 minutes at 100 RF power
 - b. Deposit Ta at 5 mT (50 SCCM Ar) for 85 seconds at 100 W DC power ~10 nm
 - c. Deposit Cu 5 mT (50 SCCM Ar) for 155 seconds at 250 W DC power ~100 nm
2. Clean sample with acetone, IPA and N₂ dry
3. Spin coat HMDS at 4000 RPM for 30 seconds
4. Spin coat AZ4210 at 4000 RPM for 60 seconds
5. Bake on 95° C hotplate for 2 minutes
6. Expose photoresist for 25 seconds with an exposure density of 5 mW/cm²
7. Develop in AZ4000K 1:4 for 2.5 to 3 minutes
8. Descum in IPC barrel etcher with O₂ at 1 Torr for 2 minute with 100 W of RF power
9. Electroplate in Cu plating solution
 - a. 93 mA forward current for 15 ms
 - b. -0.1 mA reverse current for 1 ms
 - c. Plate for 20 minutes ~2 μm
10. Strip photoresist in acetone then rinse with IPA and N₂ dry
11. Remove seed layer in Commonwealth Scientific Ion Mill
 - a. 40 mA
 - b. 500 V
 - c. -002 mA when neutralizing current is on
 - d. 7 minutes

Deposit SiO₂

1. Pre-sputter SiO₂ at 3 mTorr (60 sccm Ar) for 5 minutes with 250 W of RF power
2. Deposit SiO₂ at 3 mTorr (60 sccm Ar) for 3105 seconds with 250 W of RF power ~100 nm

Pattern Vias in SiO₂

1. Clean sample with acetone, IPA and N₂ dry
2. HMDS of #4 10 minute vapor prime at 150° C
3. Spin coat AZ4110 at 4000 RPM for 60 seconds
4. Bake on 95° C hotplate for 2 minutes
5. Expose photoresist for 30 seconds with an exposure density of 5 mW/cm²
6. Develop in AZ4000K 1:4 for 2.5 to 3 minutes
7. Etch SiO₂ in Plasma -Therm Parallel Plate RIE
 - a. CHF₃ 22.5 SCCM
 - b. O₂ 16 SCCM
 - c. 100 mTorr
 - d. 100 W RF (~350 V bias)
 - e. 2.5 minutes
 - f. Ar 20 SCCM
 - g. 20 mTorr
 - h. 20 W RF
 - i. 30 seconds
8. Rinse with acetone, IPA and dry with N₂

Electroplate Solder Bumps

1. Deposit Cu seed layer in CVC
 - a. Sputter etch sample at 5 mT (50 SCCM Ar) for 3 minutes at 100 RF power
 - b. Deposit Ta at 5 mT (50 SCCM Ar) for 85 seconds at 100 W DC power
 - c. Deposit Cu 5 mT (50 SCCM Ar) for 155 seconds at 250 W DC power
2. Clean sample with acetone, IPA and N₂ dry
3. Spin coat HMDS at 4000 RPM for 30 seconds

4. Spin coat AZ4620 at 1200 RPM for 60 seconds
5. Bake on 115° C hotplate for 4 minutes (first minute not in vacuum contact)
6. Spin coat AZ4620 at 1300 RPM for 60 seconds
7. Bake on 115° C hotplate for 4 minutes (first minute not in vacuum contact)
8. Let sample sit to rehydrate for 60 minutes
9. Expose photoresist for 3 cycles of 900 seconds with an exposure density of 5 mW/cm²
10. Let sample sit to rehydrate for 30 minutes
11. Develop in AZ4000K 1:3 for 20 to 25 minutes
12. Descum in Plasma -Therm Parallel Plate RIE
 - a. O₂ 40 SCCM
 - b. 100 mT
 - c. 100 W
 - d. 1 minute
13. Electroplate in Cu plating solution
 - a. 93 mA forward current for 15 ms
 - b. -0.1 mA reverse current for 1 ms
 - c. Plate for 100 minutes ~10 μm
14. Electroplate in Sn plating solution (Microfab Sn 200)
 - a. 93 mA forward current for 15 ms
 - b. -0.1 mA reverse current for 1 ms
 - c. Plate for 8 minutes ~10 μm
15. Strip photoresist in acetone then rinse with IPA and N₂ dry
11. Remove seed layer in Commonwealth Scientific Ion Mill (Hazardous)
 - a. Ar 1.2x10⁻⁴ Torr (~4 SCCM)
 - b. Wait 30+ minutes for gas pressure to stabilize
 - c. 10 mA and 500 V

- d. When neutralizing current is on -1 mA
- e. 15 minutes

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